

16-bit Proprietary Microcontroller

CMOS

F²MC-16F MB90210 Series

MB90214/P214A/P214B/W214A/W214B/V210

■ OUTLINE

The MB90210 series is a line of 16-bit microcontrollers particularly suitable for system control of video cameras, VTRs, and copiers. The F²MC-16F CPU integrated in this series is based on the F²MC*-16, while providing enhanced instructions for high-level languages and supporting extended addressing modes.

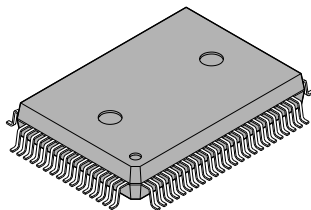
The MB90210 series incorporates a variety of peripheral resources such as a PWC timer with 4 channels, a 10-bit A/D converter with 8 channels, UART serial ports with 3 channels (1 channel for CTS and 1 channel for dual input/output pin switching), 16-bit reload timers with 8 channels, and an 8-bit PPG timer with 1 channel.

MB90P214B/W214B is under development.

*: F²MC stands for FUJITSU Flexible Microcontroller.

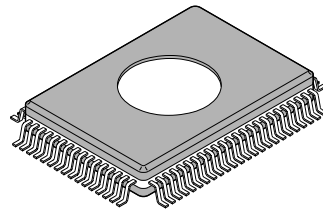
■ PACKAGE

80-pin Plastic QFP



(FPT-80P-M06)

80-pin Ceramic QFP



(FPT-80C-C02)

MB90210 Series

■ FEATURES

F²MC-16F CPU

- Minimum execution time: 62.5 ns/16-MHz oscillation (using a duty control system)
- Instruction sets optimized for controllers
 - Upward object-compatible with the F²MC-16(H)
 - Various data types (bit, byte, word, and long-word)
 - Instruction cycle improved to speed up operation
 - Extended addressing modes: 25 types
 - High coding efficiency
 - Access method (bank access with linear pointer)
 - Enhanced multiplication and division instructions (with signed instructions added)
 - Higher-precision operation using a 32-bit accumulator
- Extended intelligent I/O service (Automatic transfer function independent of instructions) access area expanded to 64 Kbytes
- Enhanced instruction set applicable to high-level language (C) and multitasking
 - System stack pointer
 - Enhanced pointer-indirect instructions
 - Barrel shift instruction
 - Stack check function
- Increased execution speed: 8-byte instruction queue
- Powerful interrupt functions: 8 levels and 29 sources

Integrated Peripheral Resources

- ROM : 64 Kbytes (MB90214)
- EPROM : 64 Kbytes (MB90W214A/W214B)
- OTPROM: 64Kbytes (MB90P214A/P214B)
- RAM: 3 Kbytes (MB90214)
 - 4 Kbytes (MB90P214A/P214B/W214A/W214B/V210)
- General-purpose ports: max. 65 channels
- PWC timer with time measurement function: 4 channels
- 10-bit A/D converter: 8 channels
- UART: 3 channels
- Including: 1 channel with CTS function
 - 1 channel with I/O pin switching function
- 16-bit reload timer
 - Toggled output, external clock, and gate functions: 4 channels
 - External clock and gate functions: 4 channels
- 8-bit PPG timer: 1 channel
- DTP/External-interrupt inputs: 4 channels
- Write-inhibit RAM: 256 bytes (MB90V210: 512 bytes)
- Timebase counter: 18 bits
- Clock gear function
- Low-power consumption mode
 - Sleep mode
 - Stop mode
 - Hardware standby mode

MB90210 Series

Product Description

- MB90214 is a mask ROM product.
- MB90P214A/P214B are OTPROM products.
- MB90W214A/W214B are EPROM products. ES only.
- Operating temperature of MB90P214A/W214A is -40°C to $+85^{\circ}\text{C}$. (However, the AC characteristics is assured in -40°C to $+70^{\circ}\text{C}$)
- MB90V210 is a evaluation device for the program development. ES only.

MB90210 Series

■ PRODUCT LINEUP

| Part number Item | MB90214 | MB90P214A MB90P214B | MB90W214A MB90W214B | MB90V210 |
|------------------------|--|------------------------|------------------------|----------------|
| Classification | Mask ROM product | OTPROM product | EPROM product | For evaluation |
| ROM size | 64 Kbytes | 64 Kbytes | 64 Kbytes | — |
| RAM size | 3 Kbytes | 4 Kbytes | 4 Kbytes | 4 Kbytes |
| CPU functions | The number of instructions: 412 Instruction bit length: 8 or 16 bits Instruction length: 1 to 7 bytes Data bit length: 1, 4, 8, 16, or 32 bits Minimum execution time: 62.5 ns/16 MHz Interrupt processing time: 1.0 μ s/16 MHz (min.) | | | |
| Ports | I/O ports (N-ch open-drain): 8 I/O ports (CMOS): 57 Total: 65 | | | |
| PWC timer | Number of channels: 4 16-bit reload timer operation (operating clock cycle: 0.25 μ s to 1.31 ms) 16-bit pulse-width count operation (Allowing continuous/one-shot measurement, H/L width measurement, inter-edge measurement, and divided-frequency measurement) | | | |
| 10-bit A/D converter | Resolution: 10 or 8 bits, Number of inputs: 8 Single conversion mode (conversion for each input channel) Scan conversion mode (continuous conversion for up to 8 consecutive channels) Continuous conversion mode (repeated conversion for a selected channel) Stop conversion mode (conversion every fixed cycle) | | | |
| UART | Number of channels: 3 (1 channel with CTS function; 1 channel with I/O pin switching function) Clock-synchronous transfer mode (full-duplex double buffering, 7- to 9-bit data length, 2400 to 62500 bps) Asynchronous transfer mode (full-duplex double buffering, 7- to 9-bit data length, 2400 to 62500 bps) | | | |
| Timer | Number of channels: 4 channels \times 2 types 16-bit reload timer operation (operating clock cycle: 0.25 μ s to 1.05 s) | | | |
| 8-bit PPG timer | Number of channels: 1 8-bit PPG operation (operating clock cycle: 0.25 μ s to 6 s) | | | |
| DTP/External interrupt | Number of inputs: 4 External interrupt mode (allowing interrupts to activate at four different request levels) Simple DMA start mode (allowing extended I ² O/S to activate at two different request levels) | | | |
| Write-inhibit RAM | RAM size: 256 bytes (MB90V210: 512 bytes) RAM write-protectable with \overline{WI} pin | | | |
| Standby mode | Stop mode (activated by software or hardware) and sleep mode | | | |
| Gear function | Machine clock operating frequency switching: 16, 8, 4, or 1 MHz (at 16 MHz oscillation) | | | |
| Package | FPT-80P-M06 | | FPT-80C-C02 | PGA-256C-A02 |

MB90210 Series

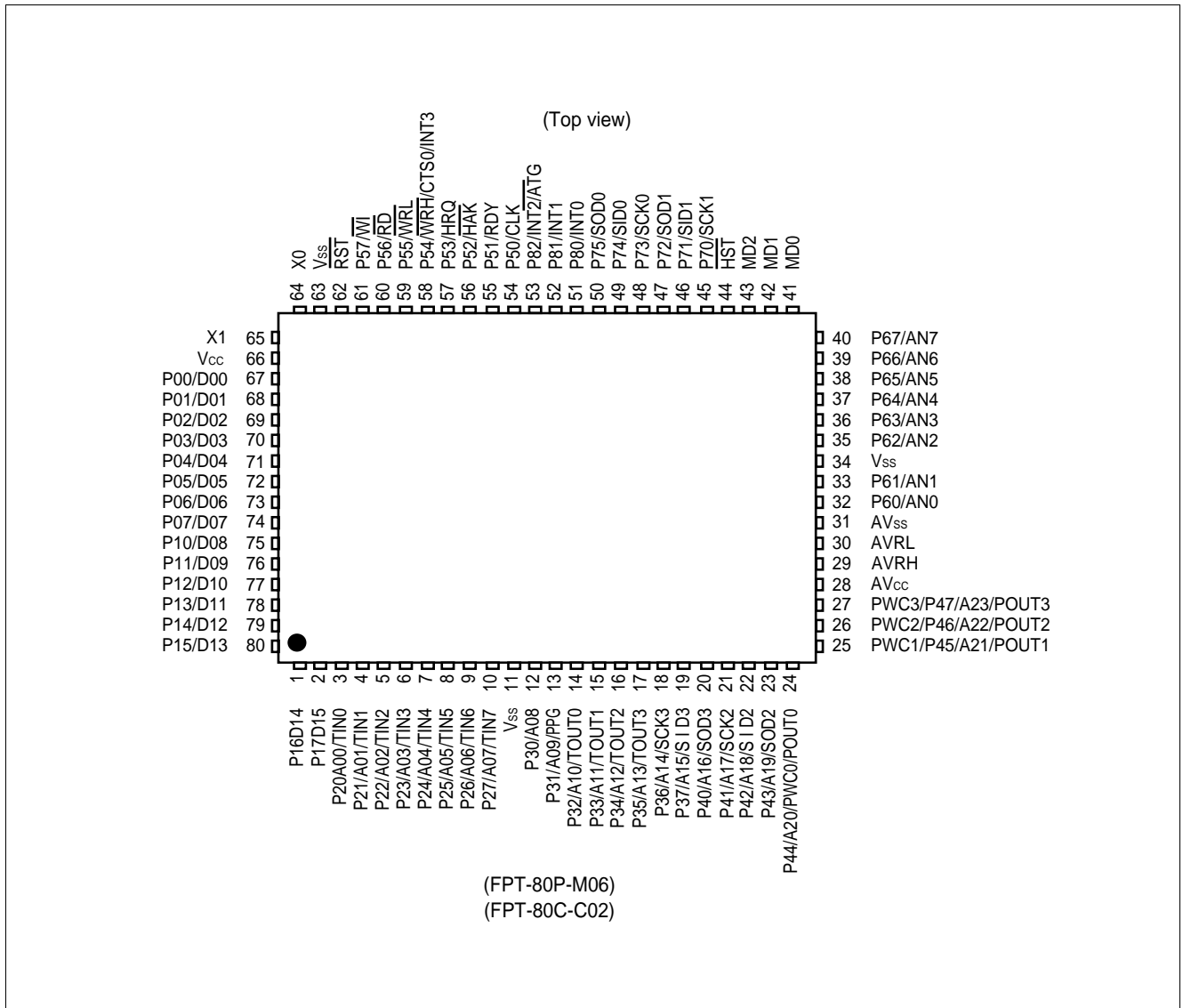
■ DIFFERENCES BETWEEN MB90214 (MASK ROM PRODUCT) AND MB90P214A/P214B/W214A/W214B

| Part number Item | MB90214 | MB90P214A MB90P214B | MB90W214A MB90W214B |
|-------------------------|-----------------------|-------------------------|------------------------|
| ROM | Mask ROM 64 Kbytes | OTPROM 64 Kbytes | EPROM 64 Kbytes |
| Pin function 43 pins | MD2 pin | MD2/V _{PP} pin | |

Note: MB90V210, device used for evaluation, is not warranted for electrical specifications.

MB90210 Series

■ PIN ASSIGNMENT



MB90210 Series

■ PIN DESCRIPTION

| Pin no. QFP* | Pin name | Circuit type | Function |
|----------------------|----------------------------|--------------|---|
| 64, 65 | X0, X1 | A | Crystal oscillator pins (16 MHz) |
| 62 | RST | H | External reset request input pin |
| 66 | V _{cc} | Power supply | Digital circuit power supply pin |
| 11, 34, 63 | V _{ss} | Power supply | Digital circuit grounding level |
| 67 to 74 | P00 to P07 | B | General-purpose I/O ports These ports are available only in the single-chip mode. |
| | D00 to D07 | | I/O pins for the lower eight bits of external data bus These pins are available in an external-bus mode. |
| 75 to 80, 1, 2 | P10 to P15, P16, P17 | B | General-purpose I/O ports These ports are available in the single-chip mode and in an external-bus mode with the 8-bit data bus specified. |
| | D08 to D13, D14, D15 | | I/O pins for the upper eight bits of external data bus These pins are available in an external-bus mode with the 16-bit data bus specified. |
| 3 to 6 | P20 to P23 | E | General-purpose I/O ports These ports are available only in the single-chip mode. |
| | A00 to A03 | | Output pins for external address buses A00 to A03 These pins are available in an external-bus mode. |
| | TIN0 to TIN3 | | 16-bit reload timer 1 (ch.0 to ch.3) input pins These pins are available when the 16-bit reload timer 1 (ch.0 to ch.3) input specification is "enabled". The data on the pin is read as the 16-bit reload timer 1 (ch.0 to ch.3) input (TIN0 to TIN3). |
| 7 to 10 | P24 to P27 | E | General-purpose I/O ports These ports are available only in the single-chip mode. |
| | A04 to A07 | | Output pins for external address buses A04 to A07 These pins are available in an external-bus mode. |
| | TIN4 to TIN7 | | 16-bit reload timer 2 (ch.4 to ch.7) input pins These pins are available when the 16-bit reload timer 2 (ch.4 to ch.7) input specification is "enabled". The data on the pin is read as the 16-bit reload timer 2 (ch.4 to ch.7) input (TIN4 to TIN7). |
| 12 | P30 | E | General-purpose I/O port This port is available in the single-chip mode or when the middle address control register setting is "port." |
| | A08 | | Output pin for external address bus A08 This pin is available in an external-bus mode and when the middle address control register set to "address." |

* : FPT-80P-M06, FPT-80C-C02

(Continued)

MB90210 Series

| Pin no. | Pin name | Circuit type | Function |
|----------|----------------|--------------|---|
| QFP* | | | |
| 13 | P31 | E | General-purpose I/O port This port is available in the single-chip mode or when the middle address control register setting is "port", with the 8-bit PPG output is disabled. |
| | A09 | | Output pin for external address bus A09 This pin is available in an external-bus mode and when the middle address control register setting is "address." |
| | PPG | | PPG timer output pin This pin is available when the PPG operation mode control register specification is the PPG output pin. |
| 14 to 17 | P32 to P35 | E | General-purpose I/O ports These ports are available in the single-chip mode or when the middle address control register setting is "port", with the 16-bit reload timer 1 (ch.0 to ch.3) output is disabled. |
| | A10 to A13 | | Output pins for external address buses A10 to A13 These pins are available in an external-bus mode and when the middle address control register setting is "address." |
| | TOUT0 to TOUT3 | | 16-bit reload timer 1 (ch.0 to ch.3) output pin These pins are available when the 16-bit reload timer 1 (ch.0 to ch.3) is output operation. |
| 18 | P36 | E | General-purpose I/O port This port is available when the UART (ch.2) clock output is disabled either in the single-chip mode or when the middle address control register setting is "port." |
| | A14 | | Output pin for external address bus A14 This pin is available when the UART (ch.2) clock output is disabled in an external-bus mode and when the middle address control register setting is "address." |
| | SCK3 | | UART (ch.2) clock output pin (SCK3) This pin is available when the UART (ch.2) clock output is enabled. UART (ch.2) external clock input pin (SCK3) This pin is available when the port is in input mode and the UART (ch.2) specification is external clock mode. |
| 19 | P37 | E | General-purpose I/O port This port is available in the single-chip mode or when the middle address control register setting is "port." |
| | A15 | | Output pin for external address bus A15 This is available in an external-bus mode and when middle address control register setting is "address." |
| | SID3 | | UART (ch.2) serial data input pin (SID3) Since this input is used whenever the SID3 is in input operation, the output by any other function must be suspended unless the output is intentionally performed. |

* : FPT-80P-M06, FPT-80C-C02

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MB90210 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|----------|--------------|---|
| 20 | P40 | E | General-purpose I/O port This port is available when the UART (ch.2) serial data output from SOD3 is disabled either in the single-chip mode or when the upper address control register setting is "port." |
| | A16 | | Output pin for external address bus A16 This pin is available when the UART (ch.2) serial data output from SOD3 is disabled in an external-bus mode and when the upper address control register setting is "address." |
| | SOD3 | | UART (ch.2) serial data output pin (SOD3) This pin is available when the UART (ch.2) serial data output is enabled. |
| 21 | P41 | E | General-purpose I/O port This port is available when the UART (ch.2) clock output is disabled either in the single-chip mode or when the upper address control register setting is "port." |
| | A17 | | Output pin for external address bus A17 This pin is available when the UART (ch.2) clock output is disabled in an external-bus mode and when the upper address control register setting is "address." |
| | SCK2 | | UART (ch.2) clock output pin (SCK2) This pin is available when the UART (ch.2) clock output is enabled. UART (ch.2) external clock input pin (SCK2) This pin is available when the port is in input mode and the UART (ch.2) specification is external clock mode. |
| 22 | P42 | E | General-purpose I/O port This port is available in the single-chip mode or when the upper address control register setting is "port." |
| | A18 | | Output pin for external address bus A18 This pin is available in an external-bus mode and when the upper address control register setting is "address." |
| | SID2 | | UART (ch.2) serial data input pin (SID2) Since this input is used whenever the SID2 is in input operation, the output by any other function must be suspended unless the output is intentionally performed. |
| 23 | P43 | E | General-purpose I/O port This port is available when the UART (ch.2) serial data output from SOD2 is disabled either in the single-chip mode or when the upper address control register setting is "port." |
| | A19 | | Output pin for external address bus A19 This pin is available when the UART (ch.2) serial data output from SOD2 is disabled in an external-bus mode and when the upper address control register setting is "address." |
| | SOD2 | | UART (ch.2) serial data output pin (SOD2) This pin is available when the UART (ch.2) serial data output from SOD2 is enabled. |

* : FPT-80P-M06, FPT-80C-C02

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MB90210 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|----------|--------------|---|
| 24 | PWC0 | E | PWC timer input pin Since this input is used whenever the PWC0 timer is in input operation, the output by any other function must be suspended unless the output is intentionally performed. |
| | POUT0 | | PWC timer output pin This pin is available when the PWC0 is output operation. |
| 25 | P45 | E | General-purpose I/O port This port is available in the single-chip mode or when the upper address control register setting is "port." |
| | A21 | | Output pin for external address bus A21 This pin is available in an external-bus mode and when the upper address control register setting is "address." |
| | PWC1 | | PWC timer data sample input pin Since this input is used whenever the PWC1 timer is in input operation, the output by any other function must be suspended unless the output is intentionally performed. |
| | POUT1 | | PWC timer output pin This pin is available when the PWC1 is output operation. |
| 26 | P46 | E | General-purpose I/O port This port is available in the single-chip mode or when the upper address control register setting is "port." |
| | A22 | | Output pin for external address bus A22 This pin is available in an external-bus mode and when the upper address control register setting is "address." |
| | PWC2 | | PWC timer input pin Since this input is used whenever the PWC2 timer is in input operation, the output by any other function must be suspended unless the output is intentionally performed. |
| | POUT2 | | PWC timer output pin This pin is available when the PWC2 is output operation. |
| 27 | P47 | E | General-purpose I/O port This port is available in the single-chip mode or when the upper address control register setting is "port." |
| | A23 | | Output pin for external address bus A23 This pin is available in an external-bus mode and when the upper address control register setting is "address." |
| | PWC3 | | PWC timer input pin Since this input is used whenever the PWC3 timer is in input operation, the output by any other function must be suspended unless the output is intentionally performed. |
| | POUT3 | | PWC timer output pin This pin is available when the PWC3 is output operation. |

* : FPT-80P-M06, FPT-80C-C02

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MB90210 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|----------|--------------|---|
| 54 | P50 | E | General-purpose I/O port This port is available in the single-chip mode and when the CLK output is disabled. |
| | CLK | | CLK output pin This pin is available in an external-bus mode with the CLK output enabled. |
| 55 | P51 | E | General-purpose I/O port This port is available in the single-chip mode or when the ready function is disable. |
| | RDY | | Ready signal input pin This pin is available in an external-bus mode and when the ready function is enabled. |
| 56 | P52 | E | General-purpose I/O port This port is available in the single-chip mode or when the hold function is disabled. |
| | HAK | | Hold acknowledge output pin This pin is available in an external-bus mode and when the hold function is enabled. |
| 57 | P53 | E | General-purpose I/O port This port is available in the single-chip mode or when the hold function is disabled in an external-bus mode. |
| | HRQ | | Hold request input pin This pin is available in an external-bus mode and when the hold function is enabled. Since this input is used during this operation at any time, the output by any other function must be suspended unless the output is intentionally performed. |
| 58 | P54 | D | General-purpose I/O port This port is available in the single-chip mode, in the external bus 8-bit mode, or when the WRH pin output is disabled. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{cc}/V_{ss} level to use these pins in input mode. |
| | CTS0 | | UART (ch.0) clear-to-send input pin Since this input is used whenever the UART (ch.0) CTS function is enabled, the output by any other function must be suspended unless the output is intentionally performed. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{cc}/V_{ss} level to use these pins in input mode. |
| | WRH | | Write strobe output pin for the upper eight bits of data bus This pin is available in the external bus 16-bit mode with the WRH pin output enabled in an external-bus mode. |

* : FPT-80P-M06, FPT-80C-C02

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MB90210 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|------------------------|----------------------------|--------------|--|
| 58 | INT3 | D | External interrupt request input pin Since this input is used whenever external interrupts are enabled, the output by any other function must be suspended unless the output is intentionally performed. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode. |
| 59 | P55 | E | General-purpose I/O port This port is available in the single-chip mode or when the \overline{WRL} pin output is disabled. |
| | \overline{WRL} | | Write strobe output pin for the lower eight bits of data bus This pin is available in an external-bus mode and when the \overline{WRL} pin output is enabled. |
| 60 | P56 | E | General-purpose I/O port This port is available in the single-chip mode. |
| | \overline{RD} | | Data bus read strobe output pin This pin is available in an external-bus mode. |
| 61 | P57 | D | General-purpose I/O port This port is always available. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode. |
| | \overline{WI} | | RAM write disable request input Since this input is used during this operation at any time, the output by any other function must be suspended unless the output is intentionally performed. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode. |
| 32, 33, 35 to 40 | P60, P61, P62 to P67 | C | Open-drain I/O ports These ports are available when the analog input enable register setting is "port." |
| | AN0, AN1, AN2 to AN7 | | 10-bit A/D converter analog input pins These pins are available when the analog input enable register setting is "analog input." |
| 41 to 43 | MD0 to MD2 | F | Operation mode select signal input pins Connect these pins directly to V_{CC} or V_{SS} . |
| 44 | \overline{HST} | G | Hardware standby input pin |
| 45 | P70 | E | General-purpose I/O port This port is available when the UART (ch.1) clock output is disabled. |

* : FPT-80P-M06, FPT-80C-C02

(Continued)

MB90210 Series

| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|-------------|--------------|--|
| 45 | SCK1 | E | <p>UART (ch.1) clock output pin This pin is available when the UART (ch.1) clock output is enabled.</p> <p>UART (ch.1) external clock input pin This pin is available when the port is in input mode and the UART (ch.1) specification is external clock mode.</p> |
| 46 | P71 | E | <p>General-purpose I/O port This port is always available.</p> |
| | SID1 | | <p>UART (ch.1) serial data input pin Since this input is used whenever the UART (ch.1) is in input operation, the output by any other function must be suspended unless the output is intentionally performed.</p> |
| 47 | P72 | E | <p>General-purpose I/O port This port is available when the UART (ch.1) serial data output is disabled.</p> |
| | SOD1 | | <p>UART (ch.1) serial data output pin This pin is available when the UART (ch.1) serial data output is enabled.</p> |
| 48 | P73 | E | <p>General-purpose I/O port This port is available when the UART (ch.0) clock output is disabled.</p> |
| | SCK0 | | <p>UART (ch.0) clock output pin This pin is available when the UART (ch.0) clock output is enabled.</p> <p>UART (ch.0) external clock input pin This pin is available when the port is in input mode and the UART (ch.0) specification is external clock mode.</p> |
| 49 | P74 | E | <p>General-purpose I/O port This port is always available.</p> |
| | SID0 | | <p>UART (ch.0) serial data input pin Since this input is used whenever the UART (ch.0) is in input operation, the output by any other function must be suspended unless the output is intentionally performed.</p> |
| 50 | P75 | E | <p>General-purpose I/O port This port is available when the UART (ch.0) serial data output is disabled.</p> |
| | SOD0 | | <p>UART (ch.0) serial data output pin This pin is available when the UART (ch.0) serial data output is enabled.</p> |
| 51, 52 | P80, P81 | D | <p>General-purpose I/O port This port is always available.</p> <p>When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode.</p> |

* : FPT-80P-M06, FPT-80C-C02

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MB90210 Series

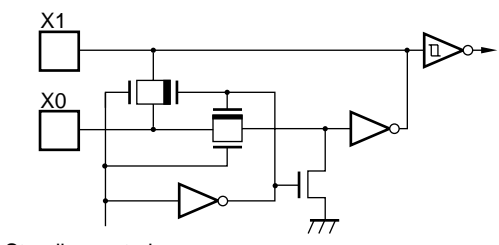
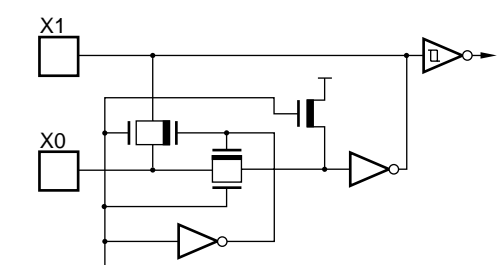
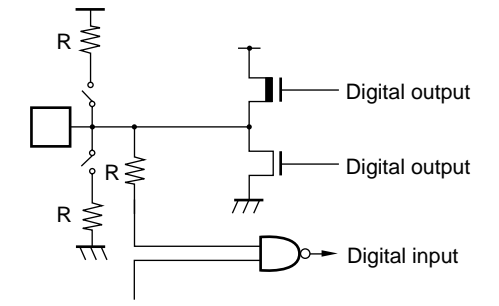
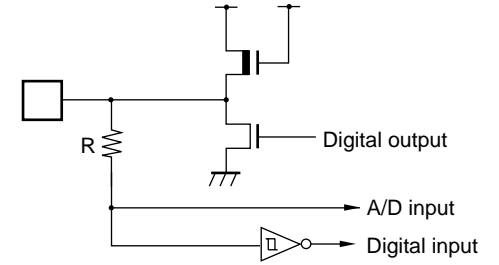
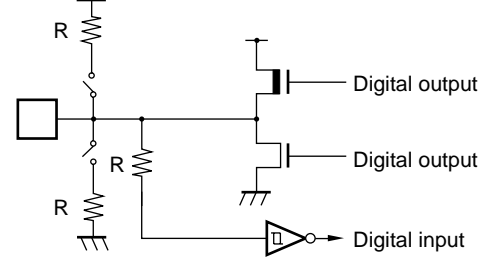
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| Pin no. QFP* | Pin name | Circuit type | Function |
|-----------------|---------------|--------------|--|
| 51, 52 | INT0, INT1 | D | External interrupt request input pin Since this input is used whenever external interrupts are enabled, the output by any other function must be suspended unless the output is intentionally performed. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode. |
| 53 | P82 | D | General-purpose I/O port This port is always available. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode. |
| | INT2 | | External interrupt request input pin Since this input is used whenever external interrupts are enabled, the output by any other function must be suspended unless the output is intentionally performed. When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode. |
| | ATG | | 10-bit A/D converter trigger input pin When these pins are open in input mode, through current may leak in stop mode/reset mode, be sure to fix these pins to V_{CC}/V_{SS} level to use these pins in input mode. |
| 28 | AV_{CC} | Power supply | Analog circuit power supply pin This power supply must be turned on or off with a potential equal to or higher than AV_{CC} applied to V_{CC} . Be sure that $AV_{CC} = V_{CC}$ before use and during operation. |
| 29 | AVRH | Power supply | Analog circuit reference voltage input pin This pins must be turned on or off with a potential equal to or higher than AVRH applied to AV_{CC} . |
| 30 | AVRL | Power supply | Analog circuit reference voltage input pin |
| 31 | AV_{SS} | Power supply | Analog circuit grounding level |

* : FPT-80P-M06, FPT-80C-C02

MB90210 Series

■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|--|--|
| A |  <p>Standby control</p> | <ul style="list-style-type: none"> Oscillation feedback resistor: Approx. 1 MΩ MB90214 MB90P214B MB90W214B |
| |  <p>Standby control</p> | <ul style="list-style-type: none"> Oscillation feedback resistor: Approx. 1 MΩ MB90P214A MB90W214A |
| B |  <p>Standby control</p> | <ul style="list-style-type: none"> CMOS-level I/O Standby control provided MB90214: With or without pull-up/pull-down resistor optional MB90P214A/P214B: Without pull-up/pull-down resistor MB90W214A/W214B: Without pull-up/pull-down resistor |
| C |  <p>Standby control</p> | <ul style="list-style-type: none"> N-ch open-drain output CMOS-level hysteresis input A/D control provided |
| D |  <p>Standby control</p> | <ul style="list-style-type: none"> CMOS-level output CMOS-level hysteresis input Standby control not provided MB90214: With or without pull-up/pull-down resistor optional MB90P214A/P214B: Without pull-up/pull-down resistor MB90W214A/W214B: Without pull-up/pull-down resistor |

(Continued)

MB90210 Series

(Continued)

| Type | Circuit | Remarks |
|------|---------|--|
| E | | <ul style="list-style-type: none"> • CMOS-level output • CMOS-level hysteresis input • Standby control provided • MB90214: With or without pull-up/pull-down resistor optional • MB90P214A/P214B: Without pull-up/pull-down resistor • MB90W214A/W214B: Without pull-up/pull-down resistor |
| F | | <ul style="list-style-type: none"> • CMOS-level input with no standby control • Mask ROM products only: • MD2: With pull-down resistor • MD1: With pull-up resistor • MD0: With pull-down resistor |
| | | <ul style="list-style-type: none"> • COMS-level input with no standby control • MD2 of OTPROM products/EPROM products only |
| G | | <ul style="list-style-type: none"> • CMOS-level hysteresis input • Standby control not provided • With input analog filter (40 ns Typ.) |
| H | | <ul style="list-style-type: none"> • CMOS-level hysteresis input • Standby control not provided • With input analog filter (40 ns Typ.) • With pull-up resistor • MB90214: With or without pull-up/pull-down resistor optional • MB90P214A/W214A/P214B/W214B: With pull-up resistor |



Note: The pull-up and pull-down resistors are always connected, regardless of the state.

■ HANDLING DEVICES

1. Preventing Latchup

CMOS ICs may cause latchup when a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins, or when a voltage exceeding the rating is applied between V_{CC} and V_{SS} .

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let any voltage exceed the maximum rating.

Also, take care to prevent the analog power supply (AV_{CC} and AV_{RH}) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Pins when A/D is not Used

Connect to be $AV_{CC} = AV_{RH} = V_{CC}$ and $AV_{SS} = AV_{RL} = V_{SS}$ even if the A/D converter is not in use.

4. Precautions when Using an External Clock

To reset the internal circuit properly by the Low-level input to the \overline{RST} pin, the "L" level input to the \overline{RST} pin must be maintained for at least five machine cycles. Pay attention to it if the chip uses external clock input.

5. V_{CC} and V_{SS} Pins

Apply equal potential to the V_{CC} and V_{SS} pins.

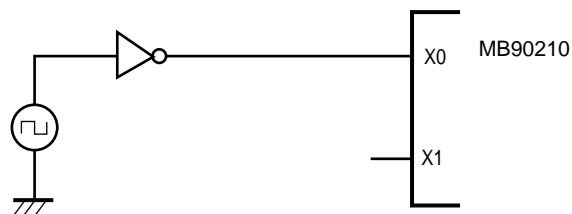
6. Supply Voltage Variation

The operation assurance range for the V_{CC} supply voltage is as given in the ratings. However, sudden changes in the supply voltage can cause misoperation, even if the voltage remains within the rated range. Therefore, it is important to supply a stable voltage to the IC. The recommended power supply control guidelines are that the commercial frequency (50 to 60 Hz) ripple variation (P-P value) on V_{CC} should be less than 10% of the standard V_{CC} value and that the transient rate of change during sudden changes, such as during power supply switching, should be less than 0.1 V/ms.

7. Notes on Using an External Clock

When using an external clock, drive the X0 pin as illustrated below. When an external clock is used, oscillation stabilization time is required even for power-on reset and wake-up from stop mode.

• Use of External Clock



Note: When using an external clock, be sure to input external clock more than 6 machine cycles after setting the HST pin to "L" to transfer to the hardware standby mode.

MB90210 Series

8. Power-on Sequence for A/D Converter Power Supplies and Analog Inputs

Be sure to turn on the digital power supply (V_{CC}) before applying voltage to the A/D converter power supplies (AV_{CC} , AV_{RH} , and AV_{RL}) and analog inputs (AN0 to AN7).

When turning power supplies off, turn off the A/D converter power supplies (AV_{CC} , AV_{RH} , and AV_{RL}) and analog inputs (AN0 to AN7) first, then the digital power supply (V_{CC}).

When turning AV_{RH} on or off, be careful not to let it exceed AV_{CC} .

MB90210 Series

■ PROGRAMMING FOR MB90P214A/P214B/W214A/W214B

In EPROM mode, the MB90P214A/P214B/W214A/W214B functions equivalent to the MBM27C1000. This allows the EPROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter (do not use the electronic signature mode).

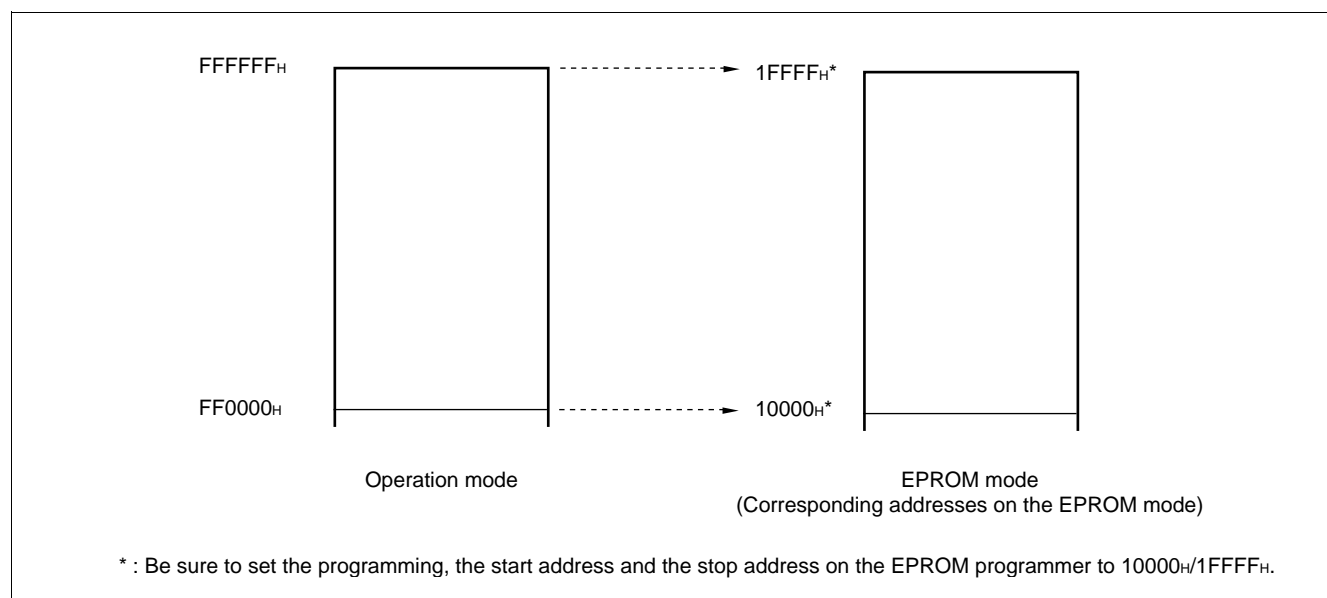
1. Program Mode

When shipped from Fujitsu, and after each erasure, all bits (64 K × 8 bits) in the MB90P214A/P214B/W214A/W214B are in the “1” state. Data is written to the ROM by selectively programming “0’s” into the desired bit locations. Bits cannot be set to “1” electrically.

2. Programming Procedure

- (1) Set the EPROM programmer to MBM27C1000.
- (2) Load program data into the EPROM programmer at 10000_H to 1FFFF_H.

Note that ROM addresses FF0000_H to FFFFFFF_H in the operation mode in the MB90P214A/P214B/W214A/W214B series assign to 10000_H to 1FFFF_H in the EPROM mode (on the EPROM programmer).



- (3) Mount the MB90P214A/P214B/W214A/W214B on the adapter socket, then fit the adapter socket onto the EPROM programmer. When mounting the device and the adapter socket, pay attention to their mounting orientations.
- (4) Start programming the program data to the device.
- (5) If programming has not successfully resulted, connect a capacitor of approx. 0.1 μF between V_{CC} and GND, between V_{PP} and GND.
- (6) Since the MB90P214A and MB90W214A have CMOS-level input, programming to them may be impossible depending on the output level of the general-purpose programmer. In that case, connect a pull-up resistor to the adapter socket side.

Note: The mask ROM products (MB90214) does not support EPROM mode. Data cannot, therefore, be read by the EPROM programmer.

MB90210 Series

3. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

| | | | |
|--|------------------------|---|-------------|
| Part No. | | MB90P214B | |
| Package | | QFP-80 | |
| Compatible socket adapter Sun Hayato Co., Ltd. | | ROM-80QF-32DP-16F | |
| Recommended programmer manufacturer and programmer name | Advantest corp. | R4945A (main unit) + R49451A (adapter) | Recommended |

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403

FAX: (81)-3-5396-9106

Advantest Corp.: TEL: Except JAPAN (81)-3-3930-4111

4. Erase Procedure

Data written in the MB90W214A/W214B are erased (from "0" to "1") by exposing the chip to ultraviolet rays with a wavelength of 2,537 Å through the translucent cover.

Recommended irradiation dosage for exposure is 10 Wsec/cm². This amount is reached in 15 to 20 minutes with a commercial ultraviolet lamp positioned 2 to 3 cm above the package (when the package surface illuminance is 1200 μW/cm²).

If the ultraviolet lamp has a filter, remove the filter before exposure. Attaching a mirrored plate to the lamp increases the illuminance by a factor of 1.4 to 1.8, thus shortening the required erasure time. If the translucent part of the package is stained with oil or adhesive, transmission of ultraviolet rays is degraded, resulting in a longer erasure time. In that case, clean the translucent part using alcohol (or other solvent not affecting the package).

The above recommended dosage is a value which takes the guard band into consideration and is a multiple of the time in which all bits can be evaluated to have been erased. Observe the recommended dosage for erasure; the purpose of the guard band is to ensure erasure in all temperature and supply voltage ranges. In addition, check the life span of the lamp and control the illuminance appropriately.

Data in the MB90W214A/W214B are erased by exposure to light with a wavelength of 4000 Å or less.

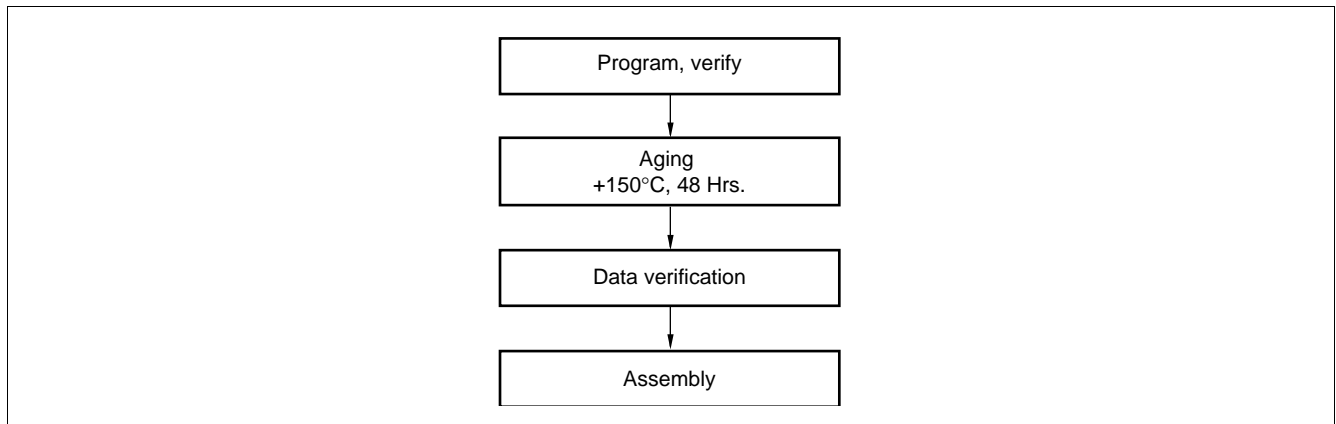
Data in the device is also erased even by exposure to fluorescent lamp light or sunlight although the exposure results in a much lower erasure rate than exposure to 2537 Å ultraviolet rays. Note that exposure to such lights for an extended period will therefore affect system reliability. If the chip is used where it is exposed to any light with a wavelength of 4000 Å or less, cover the translucent part, for example, with a protective seal to prevent the chip from being exposed to the light.

Exposure to light with a wavelength of 4,000 to 5,000 Å or more will not erase data in the device. If the light applied to the chip has a very high illuminance, however, the device may cause malfunction in the circuit for reasons of general semiconductor characteristics. Although the circuit will recover normal operation when exposure is stopped, the device requires proper countermeasures for use in a place exposed continuously to such light even though the wavelength is 4,000 Å or more.

MB90210 Series

5. Recommended Screening Conditions

High temperature aging is recommended as the pre-assembly screening procedure.



6. Programming Yield

MB90P214A/P214B cannot be write-tested for all bits due to their nature. Therefore the write yield cannot always be guaranteed to be 100%.

7. Pin Assignment in EPROM Mode

(1) Pins compatible with MBM27C1000


| MBM27C1000 | | MB90P214A, MB90P214B, MB90W214A, MB90W214B | | MBM27C1000 | | MB90P214A, MB90P214B, MB90W214A, MB90W214B | |
|------------|-----------------|---|------------------------|------------|-----------------|---|----------|
| Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name |
| 1 | V _{PP} | 43 | MD2 (V _{PP}) | 32 | V _{CC} | | |
| 2 | OE | 59 | P55 | 31 | PGM | 60 | P56 |
| 3 | A15 | 19 | P37 | 30 | N.C. | | |
| 4 | A12 | 16 | P34 | 29 | A14 | 18 | P36 |
| 5 | A07 | 10 | P27 | 28 | A13 | 17 | P35 |
| 6 | A06 | 9 | P26 | 27 | A08 | 12 | P30 |
| 7 | A05 | 8 | P25 | 26 | A09 | 13 | P31 |
| 8 | A04 | 7 | P24 | 25 | A11 | 15 | P33 |
| 9 | A03 | 6 | P23 | 24 | A16 | 20 | P40 |
| 10 | A02 | 5 | P22 | 23 | A10 | 14 | P32 |
| 11 | A01 | 4 | P21 | 22 | CE | 58 | P54 |
| 12 | A00 | 3 | P20 | 21 | D07 | 74 | P07 |
| 13 | D00 | 67 | P00 | 20 | D06 | 73 | P06 |
| 14 | D01 | 68 | P01 | 19 | D05 | 72 | P05 |
| 15 | D02 | 69 | P02 | 18 | D04 | 71 | P04 |
| 16 | GND | | | 17 | D03 | 70 | P03 |

MB90210 Series

(2) Power supply and ground connection pins

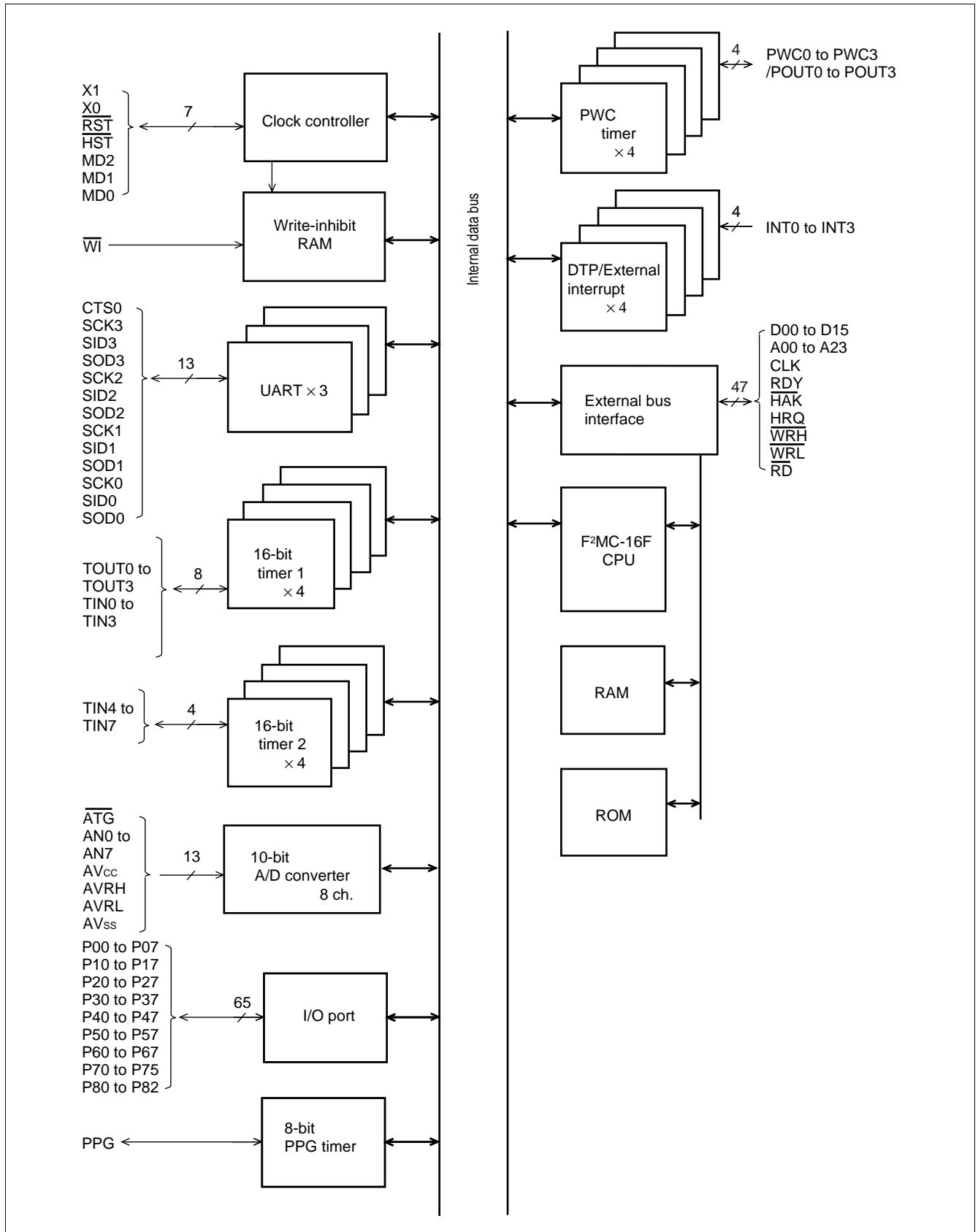
| Type | Pin no. | Pin name |
|--------------|---------|------------------|
| Power supply | 41 | MD0 |
| | 42 | MD1 |
| | 44 | FST |
| | 66 | V _{cc} |
| GND | 11 | V _{ss} |
| | 30 | AVRL |
| | 31 | AV _{ss} |
| | 34 | V _{ss} |
| | 56 | P52 |
| | 57 | P53 |
| | 62 | RST |
| | 63 | V _{ss} |

(3) Pins other than MBM27C1000-compatible pins

| Pin no. | Pin name | Treatment |
|--|---|---|
| 64 | X0 | Pull up to 4.7 k Ω . |
| 65 | X1 | Open |
| 1 2 21 to 27 28 29 32 33 35 to 40 45 to 50 51 to 53 54 55 61 75 to 80 | P16 P17 P41 to P47 AV _{cc} AVRH P60 P61 P62 to P67 P70 to P75 P80 to P82 P50 P51 P57 P10 to P15 |  <p>Connect a pull-up resistor of approximately 1 MΩ to each pin.</p> |

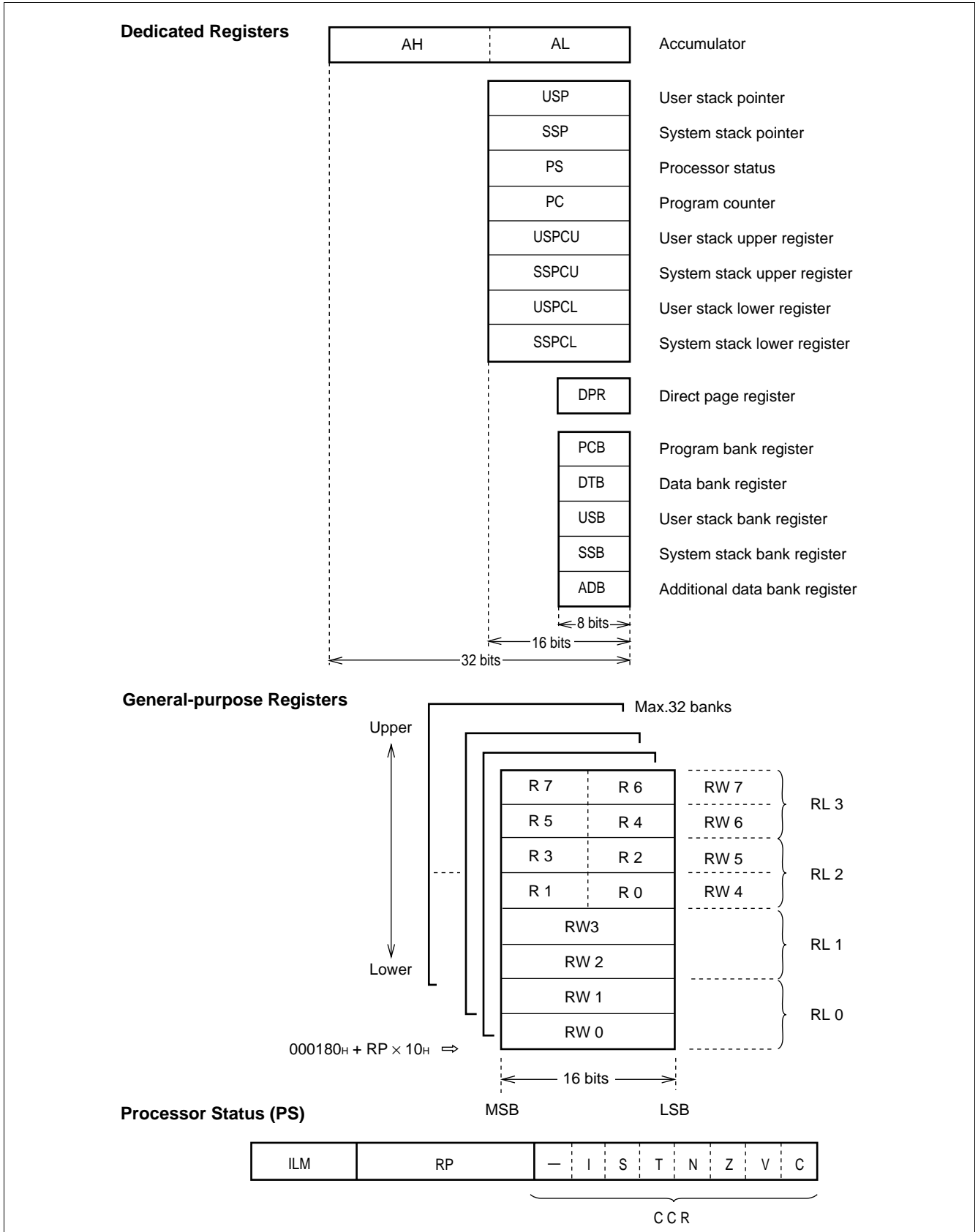
MB90210 Series

■ BLOCK DIAGRAM



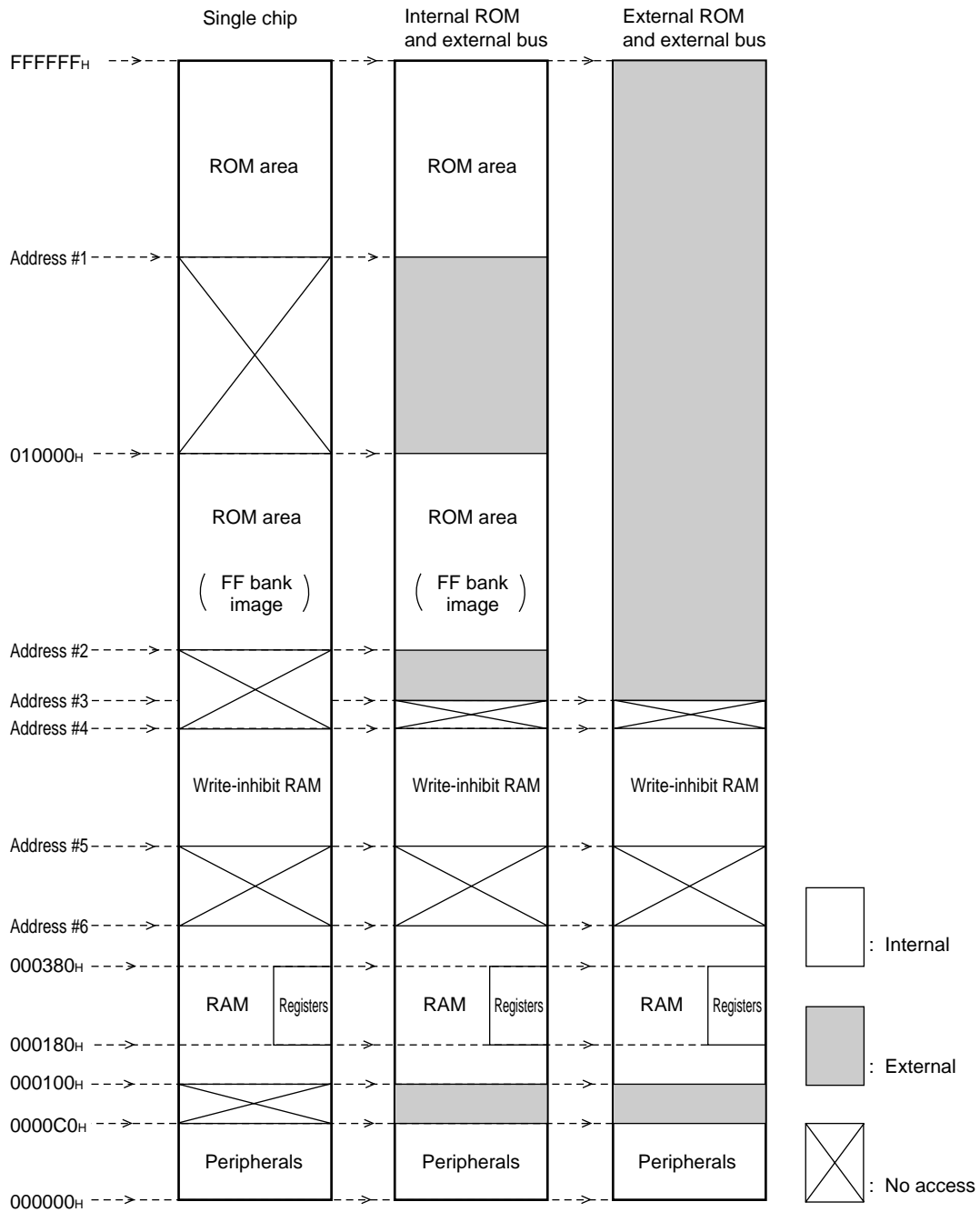
MB90210 Series

PROGRAMMING MODEL



MB90210 Series

MEMORY MAP



| Type | Address #1 | Address #2 | Address #3 | Address #4 | Address #5 | Address #6 |
|------------------------------------|------------|------------|------------|------------|------------|------------|
| MB90214 | FF0000H | 004000H | 001300H | 001200H | 001100H | 000D00H |
| MB90P214A/P214B MB90W214A/W214B | FF0000H | 004000H | 001300H | 001200H | 001100H | 001100H |
| MB90V210 | (FE0000H) | 004000H | 001300H | 001300H | 001100H | 001100H |

MB90210 Series

■ I/O MAP

| Address | Register | Register name | Access | Resource name | Initial value |
|---|--|-----------------|--------|---------------|---------------|
| 000000 _H *3 | Port 0 data register | PDR0 | R/W | Port 0 | XXXXXXXX |
| 000001 _H *3 | Port 1 data register | PDR1 | R/W | Port 1 | XXXXXXXX |
| 000002 _H *3 | Port 2 data register | PDR2 | R/W | Port 2 | XXXXXXXX |
| 000003 _H *3 | Port 3 data register | PDR3 | R/W | Port 3 | XXXXXXXX |
| 000004 _H *3 | Port 4 data register | PDR4 | R/W | Port 4 | XXXXXXXX |
| 000005 _H *3 | Port 5 data register | PDR5 | R/W | Port 5 | XXXXXXXX |
| 000006 _H | Port 6 data register | PDR6 | R/W | Port 6 | 11111111 |
| 000007 _H | Port 7 data register | PDR7 | R/W | Port 7 | --XXXXXX |
| 000008 _H | Port 8 data register | PDR8 | R/W | Port 8 | -----XXX |
| 000009 _H to 0F _H | (Reserved area) *1 | | | | |
| 000010 _H *3 | Port 0 data direction register | DDR0 | R/W | Port 0 | 00000000 |
| 000011 _H *3 | Port1 data direction register | DDR1 | R/W | Port 1 | 00000000 |
| 000012 _H *3 | Port 2 data direction register | DDR2 | R/W | Port 2 | 00000000 |
| 000013 _H *3 | Port 3 data direction register | DDR3 | R/W | Port 3 | 00000000 |
| 000014 _H *3 | Port 4 data direction register | DDR4 | R/W | Port 4 | 00000000 |
| 000015 _H *3 | Port 5 data direction register | DDR5 | R/W | Port 5 | 00000000 |
| 000016 _H | Analog input enable register | ADER | R/W | Port 6 | 11111111 |
| 000017 _H | Port 7 data direction register | DDR7 | R/W | Port 7 | --000000 |
| 000018 _H | Port 8 data direction register | DDR8 | R/W | Port 8 | -----000 |
| 000019 _H to 1F _H | (Reserved area) *1 | | | | |
| 000020 _H | Mode control register 0 | UMC0 | R/W | UART (ch.0) | 00000100 |
| 000021 _H | Status register 0 | USR0 | R/W | | 00010000 |
| 000022 _H | Input data register 0/output data register 0 | UIDR0/ UODR0 | R/W | | XXXXXXXX |
| 000023 _H | Rate and data register 0 | URD0 | R/W | | 00000000 |
| 000024 _H | Mode control register 1 | UMC1 | R/W | UART (ch.1) | 00000100 |
| 000025 _H | Status register 1 | USR1 | R/W | | 00010000 |
| 000026 _H | Input data register 1/output data register 1 | UIDR1/ UODR1 | R/W | | XXXXXXXX |
| 000027 _H | Rate and data register 1 | URD1 | R/W | | 00000000 |

(Continued)

MB90210 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---|--|-----------------|-----------|------------------------------|----------------------|
| 000028 _H | Mode control register 2 | UMC2 | R/W | UART (ch.2) | 00000100 |
| 000029 _H | Status register 2 | USR2 | R/W | | 00010000 |
| 00002A _H | Input data register 2/output data register 2 | UIDR2/ UODR2 | R/W | | XXXXXXXX |
| 00002B _H | Rate and data register 2 | URD2 | R/W | | 00000000 |
| 00002C _H | UART redirect control register | URDR | R/W | UART (ch.0/2) | ---00000 |
| 00002D _H to 2F _H | (Reserved area) *1 | | | | |
| 000030 _H | Interrupt/DTP enable register | ENIR | R/W | DTP/external interrupt | ----0000 |
| 000031 _H | Interrupt/DTP factor register | EIRR | R/W | | ----0000 |
| 000032 _H | Request level setting register | ELVR | R/W | | 00000000 |
| 000033 _H | (Reserved area) *1 | | | | |
| 000034 _H | AD control status register | ADCS | R/W | 10-bit A/D converter | 00000000 |
| 000035 _H | | | | | 00000000 |
| 000036 _H to 37 _H | AD data register | ADCD | R/W *4 | | XXXXXXXX |
| | | | | | 0-----XX |
| 000038 _H to 39 _H | Timer control status register 0 | TMCSR0 | R/W | 16-bit reload timer 1 (ch.0) | 00000000 ----0000 |
| 00003A _H to 3B _H | Timer control status register 1 | TMCSR1 | R/W | 16-bit reload timer 1 (ch.1) | 00000000 ----0000 |
| 00003C _H to 3D _H | Timer control status register 2 | TMCSR2 | R/W | 16-bit reload timer 1 (ch.2) | 00000000 ----0000 |
| 00003E _H to 3F _H | Timer control status register 3 | TMCSR3 | R/W | 16-bit reload timer 1 (ch.3) | 00000000 ----0000 |
| 000040 _H | Timer 0 timer register | TMR0 | R | 16-bit reload timer 1 (ch.0) | XXXXXXXX |
| 000041 _H | | | | | XXXXXXXX |
| 000042 _H | Timer 0 reload register | TMRLR0 | W | | XXXXXXXX |
| 000043 _H | | | | | XXXXXXXX |
| 000044 _H | Timer 1 timer register | TMR1 | R | 16-bit reload timer 1 (ch.1) | XXXXXXXX |
| 000045 _H | | | | | XXXXXXXX |
| 000046 _H | Timer 1 reload register | TMRLR1 | W | | XXXXXXXX |
| 000047 _H | | | | | XXXXXXXX |

(Continued)

MB90210 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---------------------|---------------------------------|---------------|--------|------------------------------|---------------|
| 000048 _H | Timer 2 timer register | TMR2 | R | 16-bit reload timer 1 (ch.2) | XXXXXXXX |
| 000049 _H | | | | | XXXXXXXX |
| 00004A _H | Timer 2 reload register | TMRLR2 | W | | XXXXXXXX |
| 00004B _H | | | | | XXXXXXXX |
| 00004C _H | Timer 3 timer register | TMR3 | R | 16-bit reload timer 1 (ch.3) | XXXXXXXX |
| 00004D _H | | | | | XXXXXXXX |
| 00004E _H | Timer 3 reload register | TMRLR3 | W | | XXXXXXXX |
| 00004F _H | | | | | XXXXXXXX |
| 000050 _H | Timer 4 timer register | TMR4 | R | 16-bit reload timer 2 (ch.4) | XXXXXXXX |
| 000051 _H | | | | | XXXXXXXX |
| 000052 _H | Timer 4 reload register | TMRLR4 | W | | XXXXXXXX |
| 000053 _H | | | | | XXXXXXXX |
| 000054 _H | Timer 5 timer register | TMR5 | R | 16-bit reload timer 2 (ch.5) | XXXXXXXX |
| 000055 _H | | | | | XXXXXXXX |
| 000056 _H | Timer 5 reload register | TMRLR5 | W | | XXXXXXXX |
| 000057 _H | | | | | XXXXXXXX |
| 000058 _H | Timer 6 timer register | TMR6 | R | 16-bit reload timer 2 (ch.6) | XXXXXXXX |
| 000059 _H | | | | | XXXXXXXX |
| 00005A _H | Timer 6 reload register | TMRLR6 | W | | XXXXXXXX |
| 00005B _H | | | | | XXXXXXXX |
| 00005C _H | Timer 7 timer register | TMR7 | R | 16-bit reload timer 2 (ch.7) | XXXXXXXX |
| 00005D _H | | | | | XXXXXXXX |
| 00005E _H | Timer 7 reload register | TMRLR7 | W | | XXXXXXXX |
| 00005F _H | | | | | XXXXXXXX |
| 000060 _H | Timer control status register 4 | TMCSR4 | R/W | 16-bit reload timer 2 (ch.4) | 00000000 |
| 000061 _H | (Reserved area) *1 | | | | |
| 000062 _H | Timer control status register 5 | TMCSR5 | R/W | 16-bit reload timer 2 (ch.5) | 00000000 |
| 000063 _H | (Reserved area) *1 | | | | |
| 000064 _H | Timer control status register 6 | TMCSR6 | R/W | 16-bit reload timer 2 (ch.6) | 00000000 |
| 000065 _H | (Reserved area) *1 | | | | |

(Continued)

MB90210 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|---|-------------------------------------|---------------|--------|------------------------------|---------------|
| 000066 _H | Timer control status register 7 | TMCSR7 | R/W | 16-bit reload timer 2 (ch.7) | 00000000 |
| 000067 _H | (Reserved area) *1 | | | | |
| 000068 _H | PWC0 divide ratio register | DIVR0 | R/W | PWC timer (ch.0) | -----00 |
| 000069 _H | (Reserved area) *1 | | | | |
| 00006A _H | PWC1 divide ratio register | DIVR1 | R/W | PWC timer (ch.1) | -----00 |
| 00006B _H | (Reserved area) *1 | | | | |
| 00006C _H | PWC2 divide ratio register | DIVR2 | R/W | PWC timer (ch.2) | -----00 |
| 00006D _H | (Reserved area) *1 | | | | |
| 00006E _H | PWC3 divide ratio register | DIVR3 | R/W | PWC timer (ch.3) | -----00 |
| 00006F _H | (Reserved area) *1 | | | | |
| 000070 _H | PWC0 control status register | PWCSR0 | R/W | PWC timer (ch.0) | 00000000 |
| 000071 _H | | | | | 00000000 |
| 000072 _H | PWC0 data buffer register | PWCR0 | R/W | | 00000000 |
| 000073 _H | | | | | 00000000 |
| 000074 _H | PWC1 control status register | PWCSR1 | R/W | PWC timer (ch.1) | 00000000 |
| 000075 _H | | | | | 00000000 |
| 000076 _H | PWC1 data buffer register | PWCR1 | R/W | | 00000000 |
| 000077 _H | | | | | 00000000 |
| 000078 _H | PWC2 control status register | PWCSR2 | R/W | PWC timer (ch.2) | 00000000 |
| 000079 _H | | | | | 00000000 |
| 00007A _H | PWC2 data buffer register | PWCR2 | R/W | | 00000000 |
| 00007B _H | | | | | 00000000 |
| 00007C _H | PWC3 control status register | PWCSR3 | R/W | PWC timer (ch.3) | 00000000 |
| 00007D _H | | | | | 00000000 |
| 00007E _H | PWC3 data buffer register | PWCR3 | R/W | | 00000000 |
| 00007F _H | | | | | 00000000 |
| 000080 _H to 87 _H | (Reserved area) *1 | | | | |
| 000088 _H | PPG operation mode control register | PPGC | R/W | 8-bit PPG timer | 0000--1 |
| 000089 _H | (Reserved area) *1 | | | | |

(Continued)

MB90210 Series

| Address | Register | Register name | Access | Resource name | Initial value |
|-------------------|--|---------------|--------|--|---------------|
| 00008AH | PPG reload register | PRL | R/W | 8-bit PPG timer | XXXXXXXX |
| 00008BH | | | | | XXXXXXXX |
| 00008CH to 8DH | (Reserved area) *1 | | | | |
| 00008EH | WI control register | WICR | R/W | Write-inhibit RAM | ---X--- |
| 00008FH to 9EH | (Reserved area) *1 | | | | |
| 00009FH | Delayed interrupt source generate/ release register | DIRR | R/W | Delayed interrupt generation module | -----0 |
| 0000A0H | Standby control register | STBYC | R/W | Low-power consumption mode | 0001**** |
| 0000A1H to A2H | (Reserved area) *1 | | | | |
| 0000A3H | Middle address control register | MACR | W | External pin | ##### |
| 0000A4H | Upper address control register | HACR | W | | ##### |
| 0000A5H | External pin control register | EPCR | W | | ##0-0#00 |
| 0000A6H to A7H | (Reserved area) *1 | | | | |
| 0000A8H | Watchdog timer control register | WTC | R/W | Watchdog timer | XXXXXXXX |
| 0000A9H | Timebase timer control register | TBTC | R/W | Timebase timer | 1--00000 |
| 0000AAH to AFH | (Reserved area) *1 | | | | |
| 0000B0H | Interrupt control register 00 | ICR00 | R/W | Interrupt controller | 00000111 |
| 0000B1H | Interrupt control register 01 | ICR01 | R/W | | 00000111 |
| 0000B2H | Interrupt control register 02 | ICR02 | R/W | | 00000111 |
| 0000B3H | Interrupt control register 03 | ICR03 | R/W | | 00000111 |
| 0000B4H | Interrupt control register 04 | ICR04 | R/W | | 00000111 |
| 0000B5H | Interrupt control register 05 | ICR05 | R/W | | 00000111 |
| 0000B6H | Interrupt control register 06 | ICR06 | R/W | | 00000111 |
| 0000B7H | Interrupt control register 07 | ICR07 | R/W | | 00000111 |
| 0000B8H | Interrupt control register 08 | ICR08 | R/W | | 00000111 |
| 0000B9H | Interrupt control register 09 | ICR09 | R/W | | 00000111 |

(Continued)

MB90210 Series

(Continued)

| Address | Register | Register name | Access | Resource name | Initial value |
|---|-------------------------------|---------------|--------|----------------------|---------------|
| 0000BA _H | Interrupt control register 10 | ICR10 | R/W | Interrupt controller | 00000111 |
| 0000BB _H | Interrupt control register 11 | ICR11 | R/W | | 00000111 |
| 0000BC _H | Interrupt control register 12 | ICR12 | R/W | | 00000111 |
| 0000BD _H | Interrupt control register 13 | ICR13 | R/W | | 00000111 |
| 0000BE _H | Interrupt control register 14 | ICR14 | R/W | | 00000111 |
| 0000BF _H | Interrupt control register 15 | ICR15 | R/W | | 00000111 |
| 0000C0 _H to FF _H | (External area) *2 | | | | |

Initial value

0: The initial value of this bit is 0.

1: The initial value of this bit is 1.

X: The initial value of this bit is undefined.

–: This bit is not used. The initial value is undefined.

*: The initial value of this bit varies with the reset source.

#: The initial value of this bit varies with the operation mode.

*1: Access inhibited

*2: The only area available for the external access below address 0000FF_H is this area. Accesses to these addresses are handled as accesses to an external I/O area.

*3: When the external bus is enabled, do not access any register not serving as a general-purpose port in the areas from address 000000_H to 000005_H and from 000010_H to 000015_H.

*4: Writing to bit 15 is possible. Writing to other bits is used as a test function.

MB90210 Series

■ INTERRUPT SOURCES AND INTERRUPT VECTORS/INTERRUPT CONTROL REGISTERS

| Interrupt source | EI ² OS support | Interrupt vector | | | Interrupt control register | |
|------------------------------------|----------------------------|------------------|-----------------|---------------------|----------------------------|--------------------|
| | | No. | Address | Address | ICR | Address |
| Reset | × | # 08 | 08 _H | FFFFDC _H | — | — |
| INT9 instruction | × | # 09 | 09 _H | FFFFD8 _H | — | — |
| Exceptional | × | # 10 | 0A _H | FFFFD4 _H | — | — |
| UART interrupt #0 | △ | # 11 | 0B _H | FFFFD0 _H | ICR00 | 000B0 _H |
| UART interrupt #1 | △ | # 12 | 0C _H | FFFFCC _H | | |
| UART interrupt #2 | △ | # 13 | 0D _H | FFFFC8 _H | ICR01 | 000B1 _H |
| UART interrupt #3 | △ | # 14 | 0E _H | FFFFC4 _H | | |
| PWC timer # 0 · count completed | △ | # 15 | 0F _H | FFFFC0 _H | ICR02 | 000B2 _H |
| PWC timer # 0 · overflow | △ | # 16 | 10 _H | FFFFBC _H | | |
| PWC timer # 1 · count completed | △ | # 17 | 11 _H | FFFFB8 _H | ICR03 | 000B3 _H |
| PWC timer # 1 · overflow | △ | # 18 | 12 _H | FFFFB4 _H | | |
| PWC timer # 2 · count completed | △ | # 19 | 13 _H | FFFFB0 _H | ICR04 | 000B4 _H |
| PWC timer # 2 · overflow | △ | # 20 | 14 _H | FFFFAC _H | | |
| PWC timer # 3 · count completed | △ | # 21 | 15 _H | FFFFA8 _H | ICR05 | 000B5 _H |
| PWC timer # 3 · overflow | △ | # 22 | 16 _H | FFFFA4 _H | | |
| 16-bit reload timer 1 # 0 overflow | △ | # 23 | 17 _H | FFFFA0 _H | ICR06 | 000B6 _H |
| 16-bit reload timer 1 # 1 overflow | △ | # 24 | 18 _H | FFFF9C _H | | |
| 16-bit reload timer 1 # 2 overflow | △ | # 25 | 19 _H | FFFF98 _H | ICR07 | 000B7 _H |
| 16-bit reload timer 1 # 3 overflow | △ | # 26 | 1A _H | FFFF94 _H | | |
| 16-bit reload timer 2 # 4 overflow | △ | # 27 | 1B _H | FFFF90 _H | ICR08 | 000B8 _H |
| 16-bit reload timer 2 # 5 overflow | △ | # 28 | 1C _H | FFFF8C _H | | |
| 16-bit reload timer 2 # 6 overflow | △ | # 29 | 1D _H | FFFF88 _H | ICR09 | 000B9 _H |
| 16-bit reload timer 2 # 7 overflow | △ | # 30 | 1E _H | FFFF84 _H | | |
| A/D converter count completed | △ | # 31 | 1F _H | FFFF80 _H | ICR10 | 000BA _H |
| Timebase timer interval interrupt | △ | # 32 | 20 _H | FFFF7C _H | | |
| UART2 · transmission completed | △ | # 33 | 21 _H | FFFF78 _H | ICR11 | 000BB _H |
| UART2 · reception completed | △ | # 34 | 22 _H | FFFF74 _H | | |

(Continued)

MB90210 Series

(Continued)

| Interrupt source | EI ² OS support | Interrupt vector | | | Interrupt control register | |
|-------------------------------------|----------------------------|------------------|-----------------|---------------------|----------------------------|---------------------|
| | | No. | Address | Address | ICR | Address |
| UART1 · transmission completed | ○ | # 35 | 23 _H | FFFF70 _H | ICR12 | 0000BC _H |
| UART1 · reception completed | ○ | # 36 | 24 _H | FFFF6C _H | | |
| UART0 · transmission completed | ◎ | # 37 | 25 _H | FFFF68 _H | ICR13 | 0000BD _H |
| UART0 · reception completed | ◎ | # 39 | 27 _H | FFFF60 _H | ICR14 | 0000BE _H |
| Delayed interrupt generation module | × | # 42 | 2A _H | FFFF54 _H | ICR15 | 0000BF _H |
| Stack fault | × | # 255 | FF _H | FFFC00 _H | — | — |

◎: EI²OS is supported (with stop request).

○: EI²OS is supported; however, since two interrupt sources are allocated to a single ICR, in case EI²OS is used for one of the two, EI²OS and ordinary interrupt are not both available for the other (with stop request).

△: EI²OS is supported; however, since two interrupt sources are allocated to a single ICR, in case EI²OS is used for one of the two, EI²OS and ordinary interrupt are not both available for the other (with no stop request).

×: EI²OS is not supported.

MB90210 Series

■ PERIPHERAL RESOURCES

1. Parallel Ports

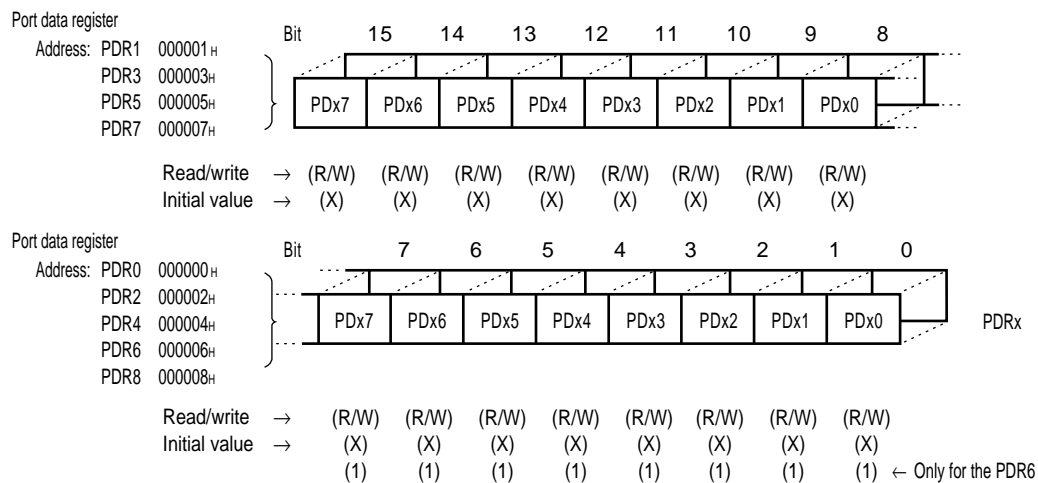
The MB90210 series has 57 I/O pins and 8 open-drain I/O pins.

Ports 0 to 5, 7, and 8 are I/O ports. Each of these ports serves as an input port when the data direction register value is 0 and as an output port when the value is 1.

Port 6 is an open-drain port, which may be used as a port when the analog input enable register value is 0.

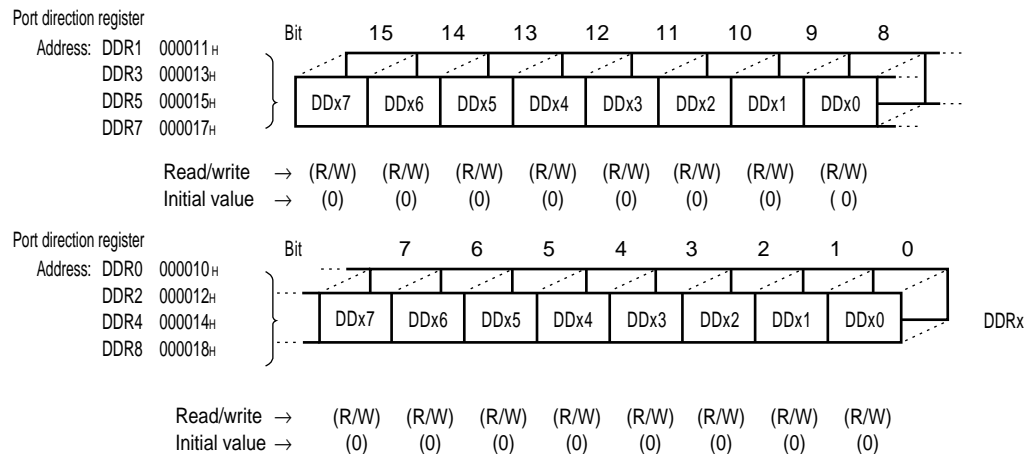
(1) Register Configuration

• Port data registers 0 to 8 (PDR0 to PDR8)



Note: No register bit is included in bits 7 and 6 of port 7 or bits 7 to 3 of port 8.

• Port direction registers 0 to 5, 7, and 8 (DDR0 to DDR5, DDR7, and DDR8)



Note: No register bit is included in bits 7 and 6 of port 7 or bits 7 to 3 of port 8.
Port 6 has no DDR.

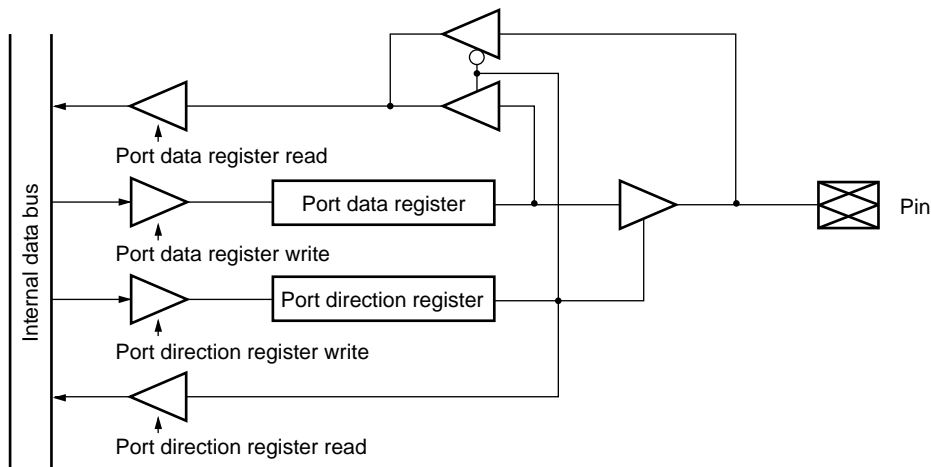
MB90210 Series

- Analog input enable register (ADER)

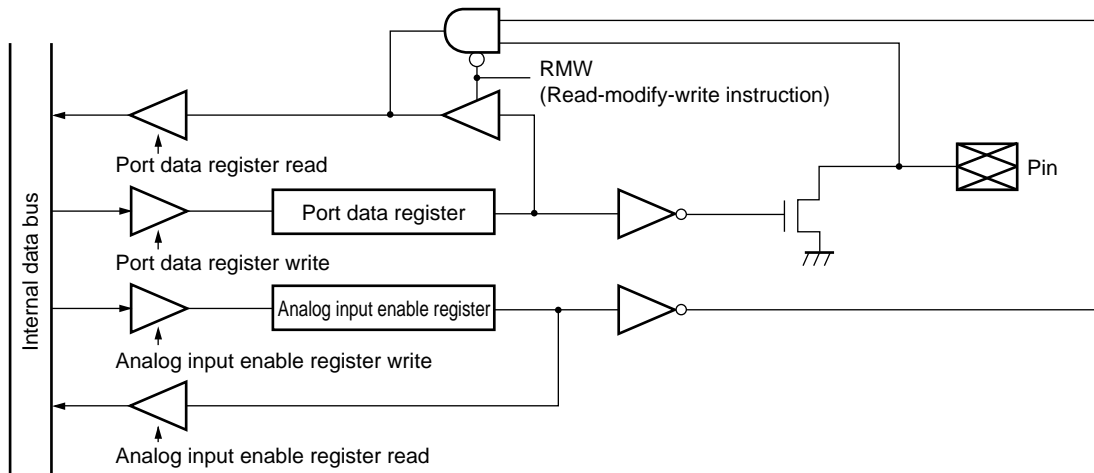
| Analog input enable register | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-----------------------------------|--|-----|-------|-------|-------|-------|-------|-------|-------|-------|------|
| Address: ADER 000016 _H | | | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 | ADER |
| Read/write → | | | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |
| Initial value → | | | (1) | (1) | (1) | (1) | (1) | (1) | (1) | (1) | |

(2) Block Diagram

- I/O port (Port 0 to 5, 7, and 8)



- I/O port with an open-drain output (Port 6)



MB90210 Series

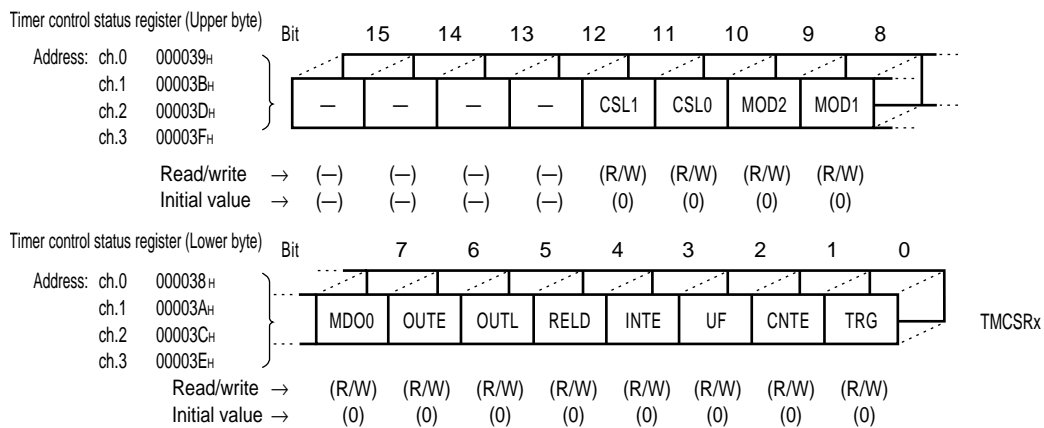
2. 16-bit Reload Timer 1 (with Event Count Function)

The 16-bit reload timer 1 consists of a 16-bit down counter, a 16-bit reload register, an input pin (TIN), an output pin (TOUT), and a control register. The input clock can be selected from among three internal clocks and one external clock. At the output pin (TOUT), the pulses in the toggled output waveform are output in the reload mode; the rectangular pulses indicating that the timer is counting are in the single-shot mode. The input pin (TIN) can be used for event input in the event count mode, and for trigger input or gate input in the internal clock mode.

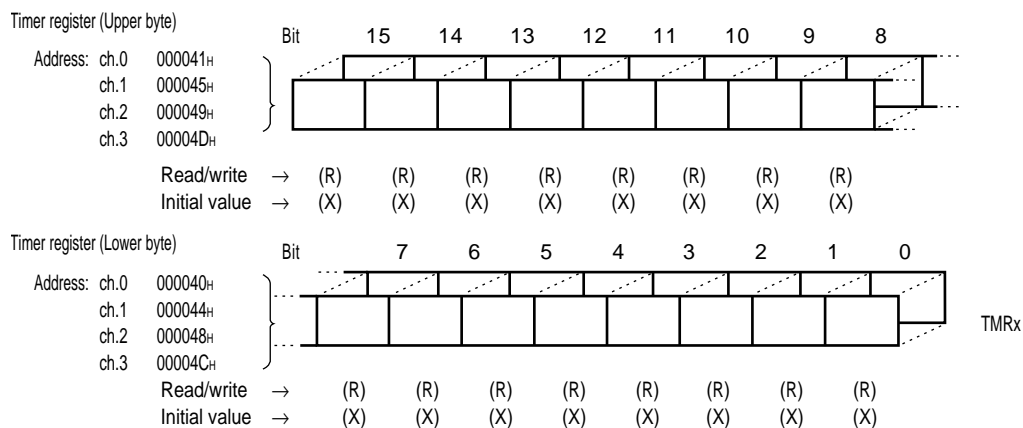
MB90210 series contains four channels for this timer.

(1) Register Configuration

• Timer control status register (TMCSR)

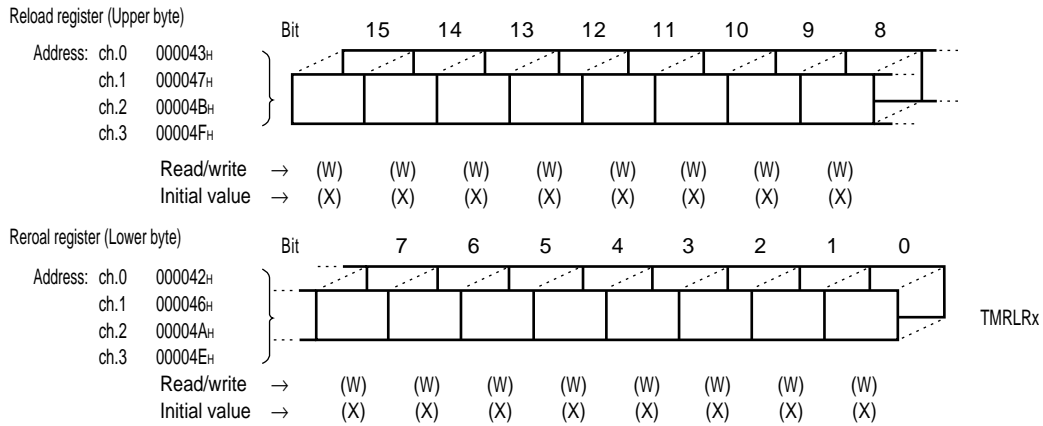


• Timer register (TMR)

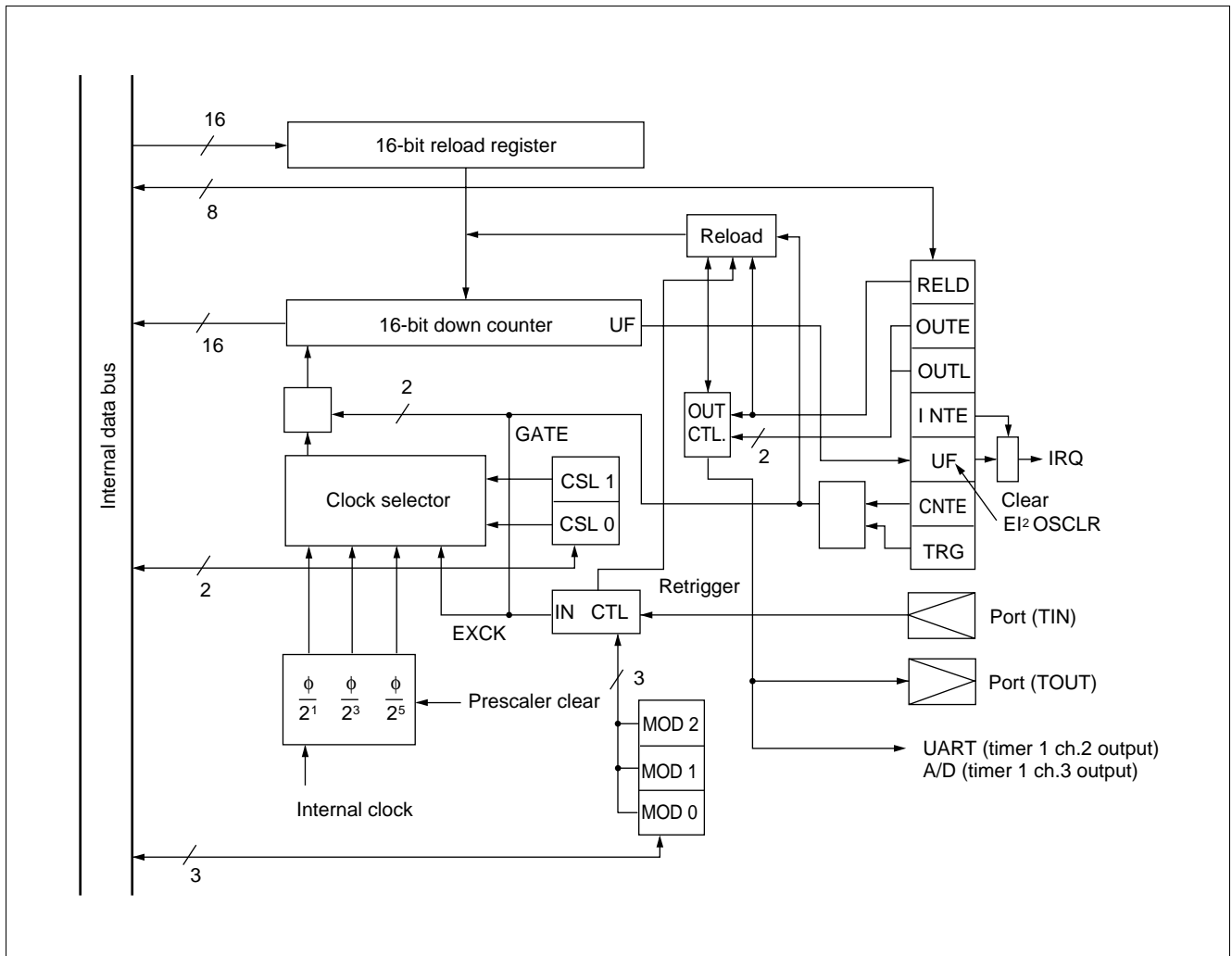


MB90210 Series

• Reload register (TMRLR)



(2) Block Diagram



MB90210 Series

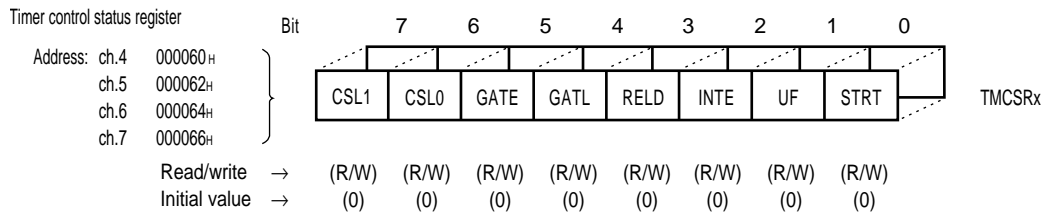
3. 16-bit Reload Timer 2 (with Gate Mode)

The 16-bit reload timer 2 consists of a 16-bit down counter, a 16-bit reload register, an input pin (TIN), and an 8-bit control register. The input clock can be selected from among four internal clocks.

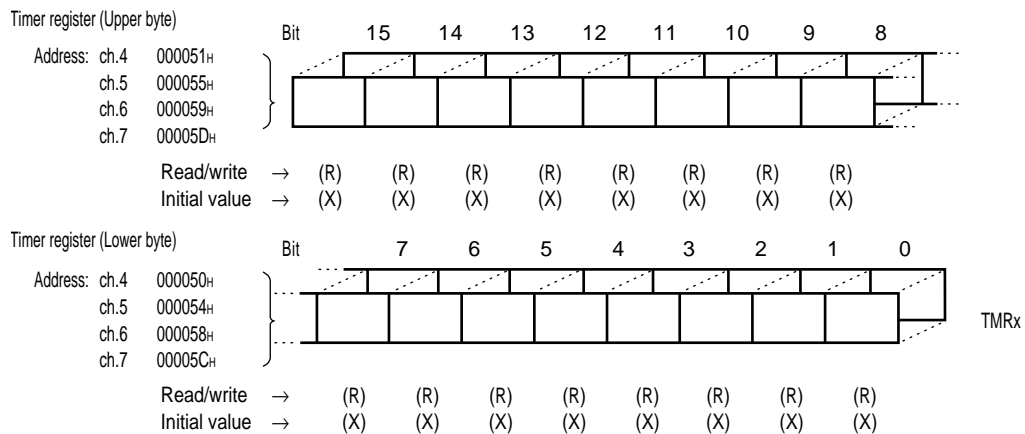
The MB90210 series contains four channels for this timer.

(1) Register Configuration

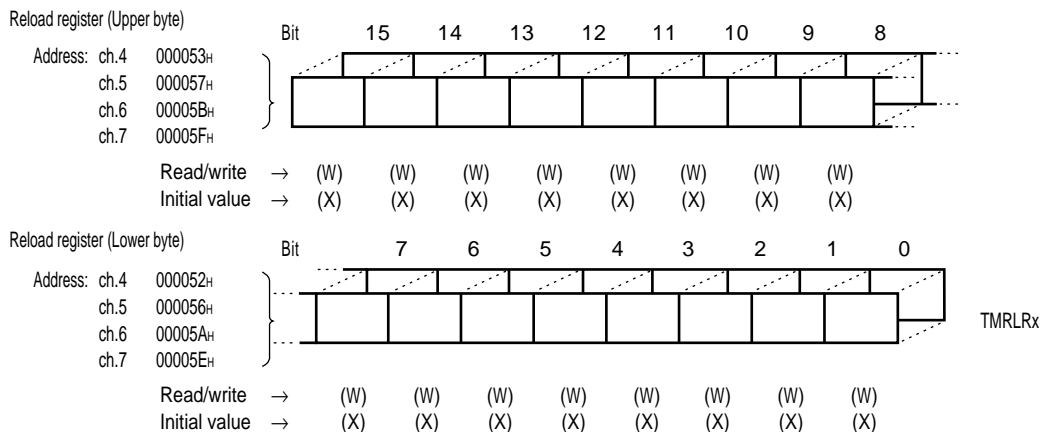
• Timer control status register (TMCSR)



• Timer register (TMR)

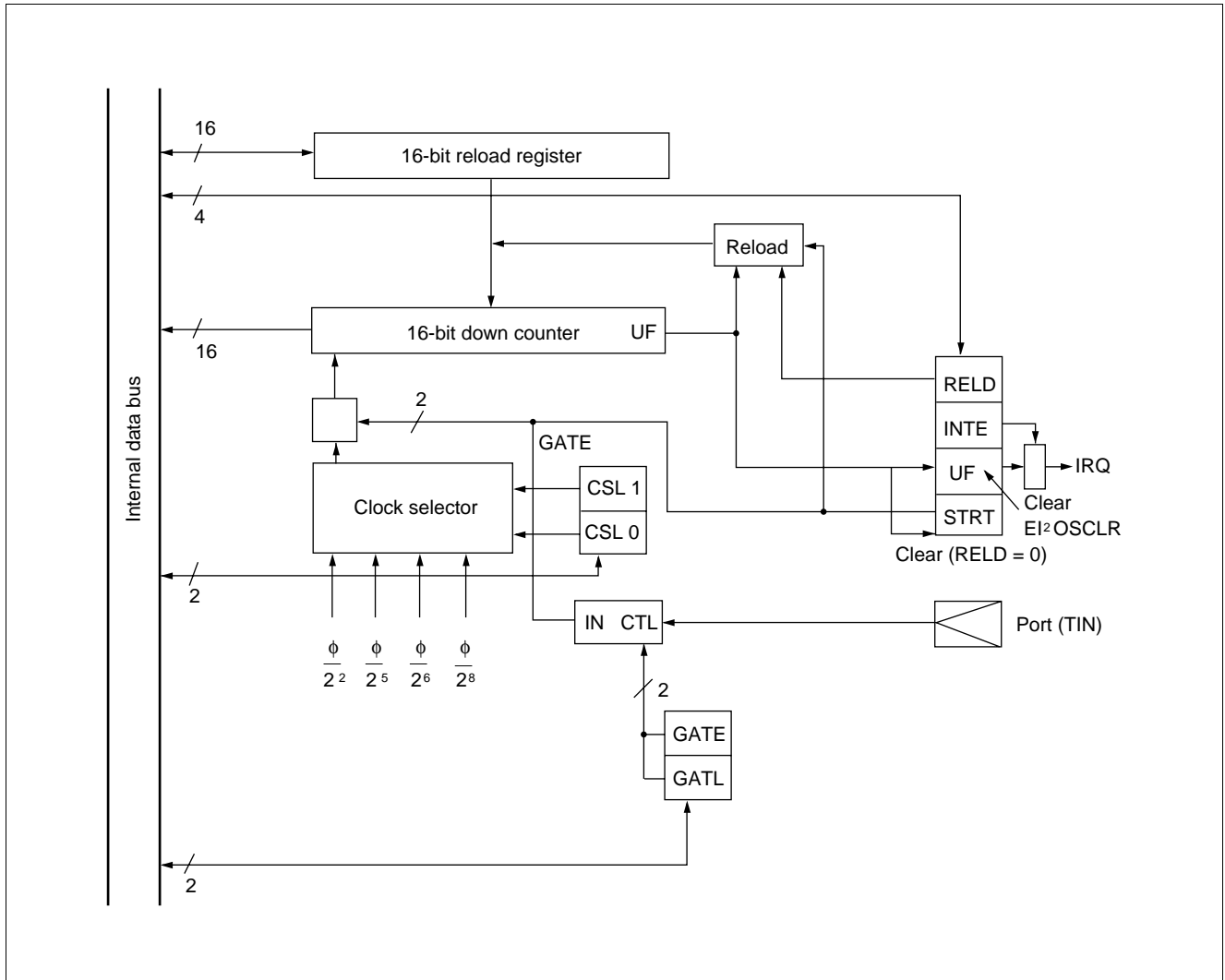


• Reload register (TMRLR)



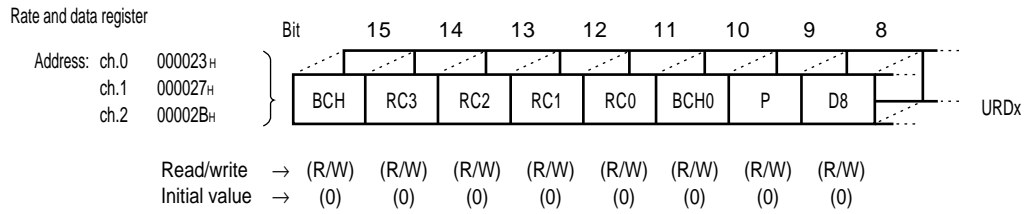
MB90210 Series

(2) Block Diagram

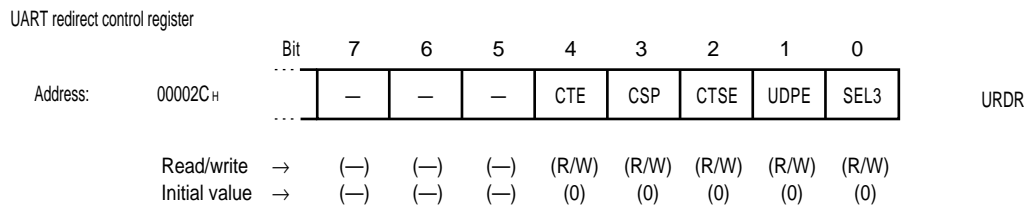


MB90210 Series

• Rate and data register (URD)

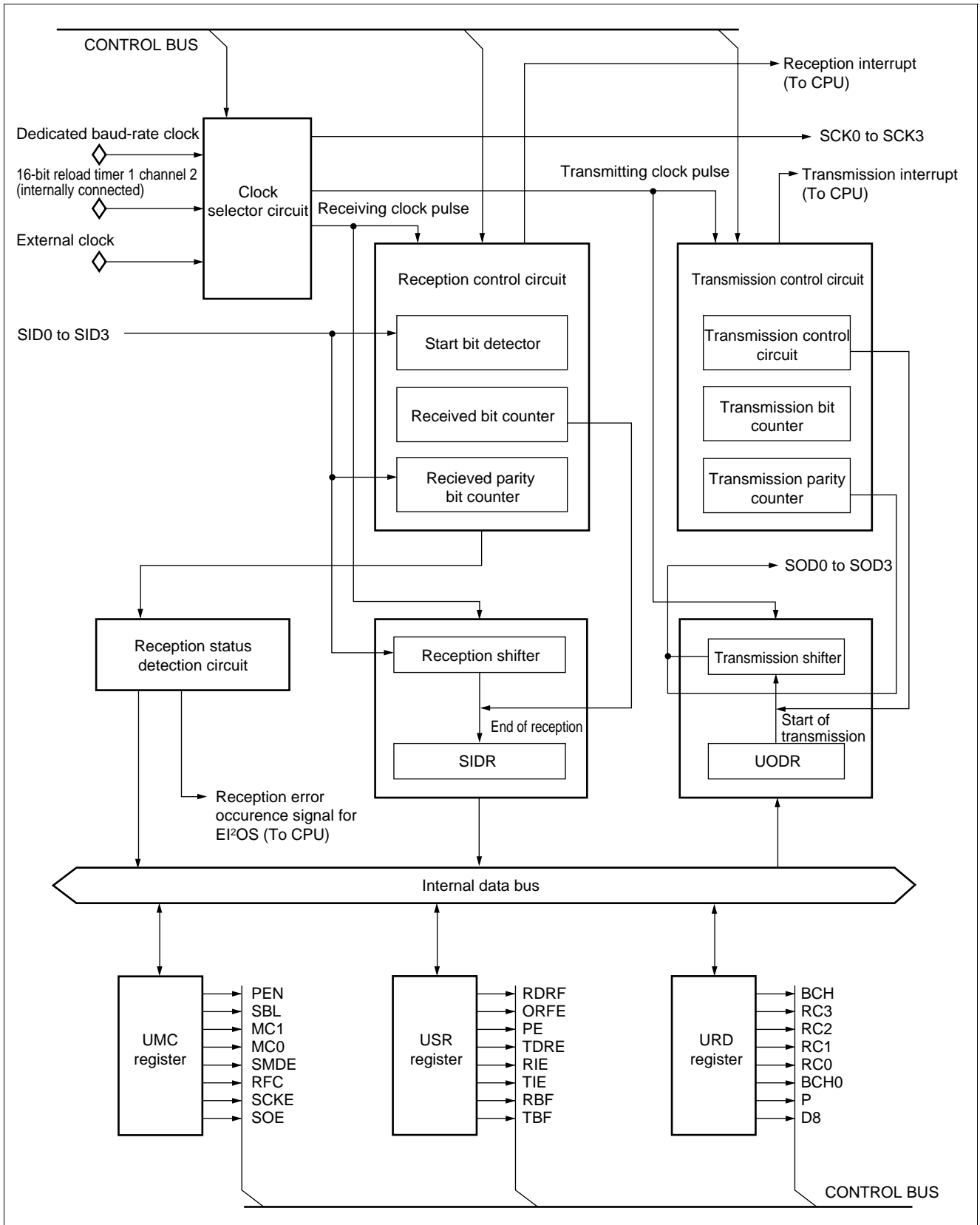


• UART redirect control register (URDR)



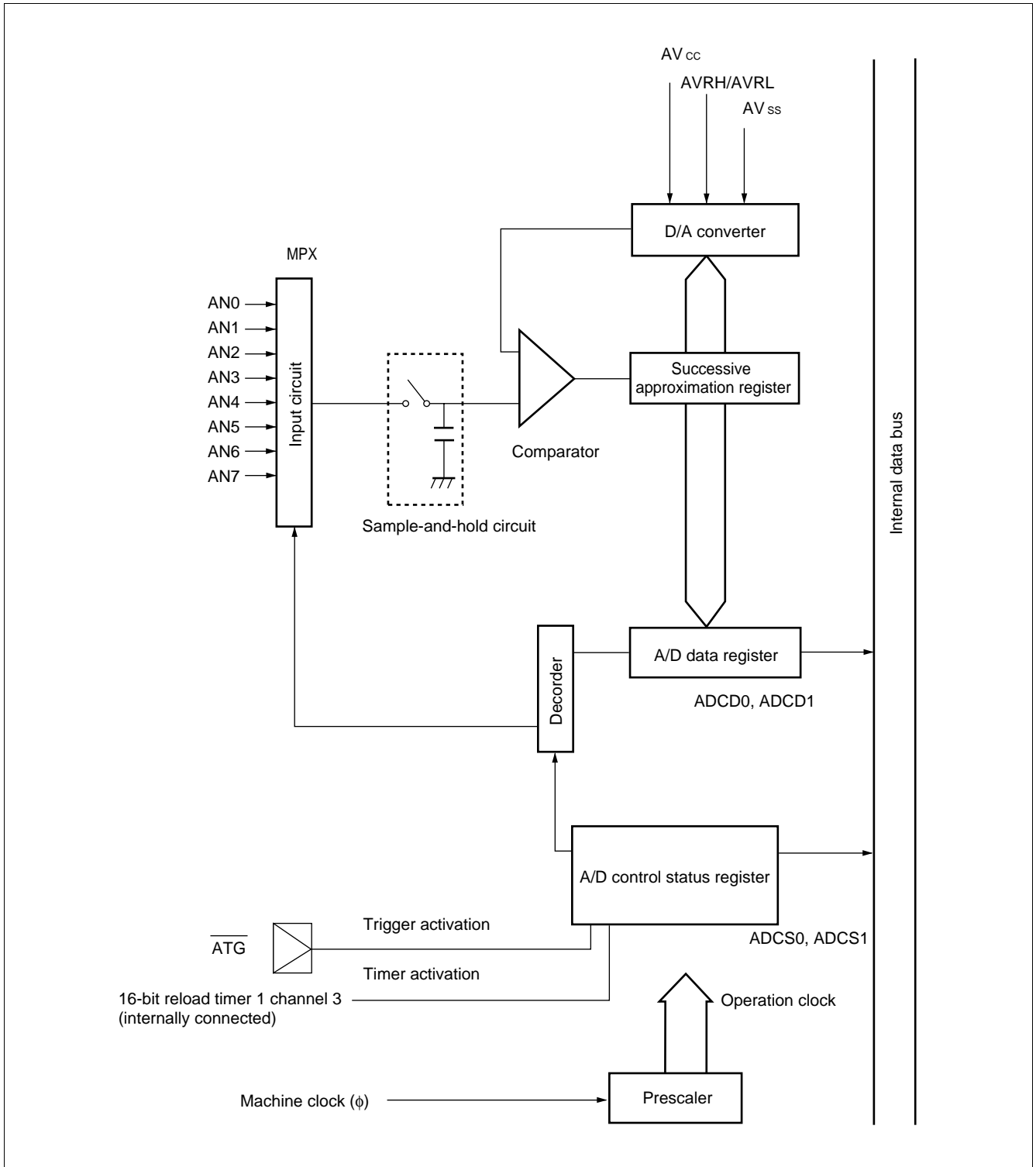
MB90210 Series

(2) Block Diagram



MB90210 Series

(2) Block Diagram



6. PWC(Pulse Width Count) Timer

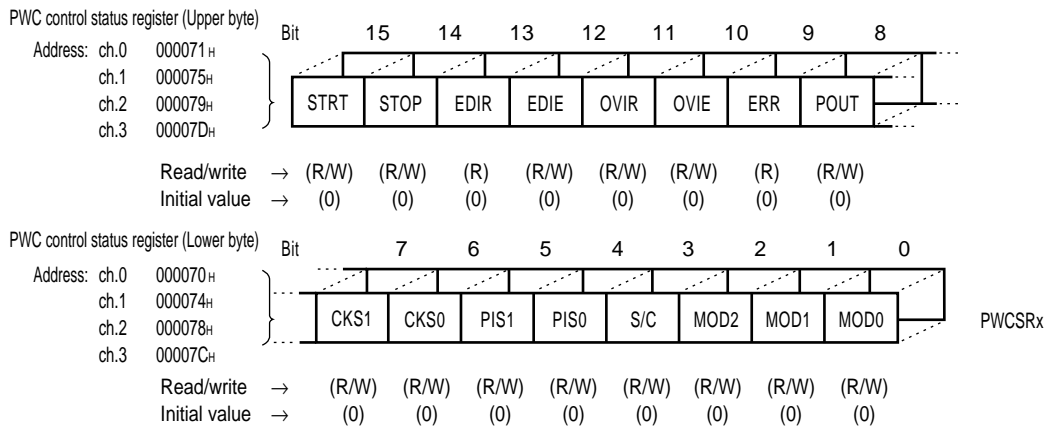
The PWC (pulse width count) timer is a 16-bit multifunction up-count timer with an input-signal pulse-width count function and a reload timer function. The hardware configuration of this module is a 16-bit up-count timer, an input pulse divider with divide ratio control register, four count input pins, and a 16-bit control register. Using these components, the PWC timer provides the following features:

- Timer functions:
 - An interrupt request can be generated at set time intervals.
 - Pulse signals synchronized with the timer cycle can be output.
 - The reference internal clock can be selected from among three internal clocks.
- Pulse-width count functions:
 - The time between arbitrary pulse input events can be counted.
 - The reference internal clock can be selected from among three internal clocks.
 - Various count modes:
 - “H” pulse width (\uparrow to \downarrow) / “L” pulse width (\uparrow to \downarrow)
 - Rising-edge cycle (\uparrow to \uparrow) / Falling-edge cycle (\downarrow to \downarrow)
 - Count between edges (\uparrow or \downarrow to \downarrow or \uparrow)
 - Cycle count can be performed by $22n$ division ($n = 1, 2, 3, 4$) of the input pulse, with an 8 bit input divider.
 - An interrupt request can be generated once counting has been performed.
 - The number of times counting is to be performed (once or subsequently) can be selected.

The MB90210 series contains four channels for the PWC timer.

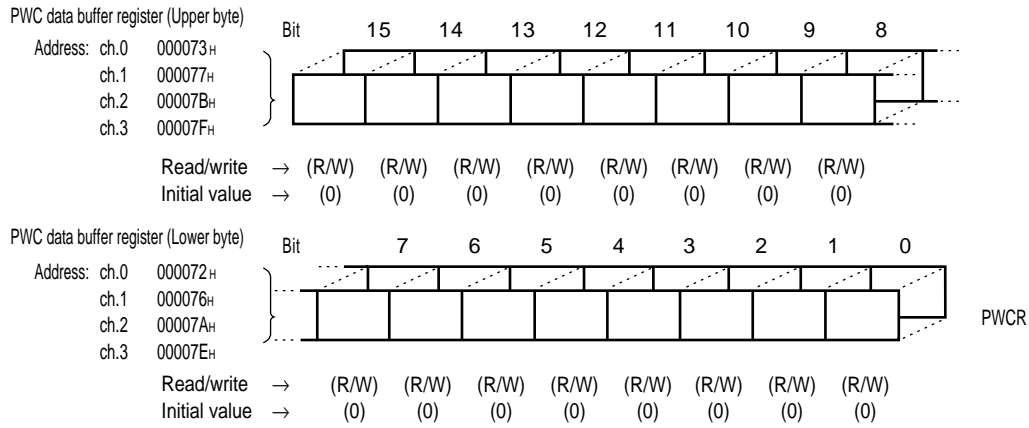
(1) Register Configuration

• PWC control status register (PWCSR)

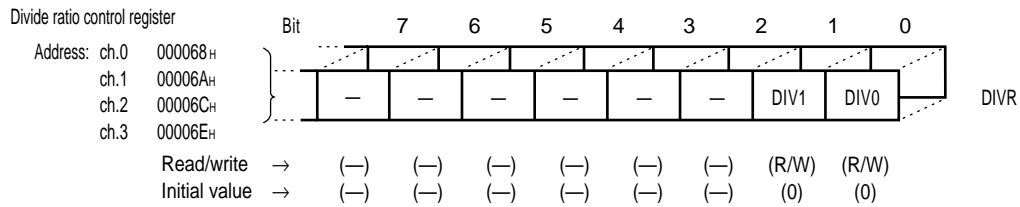


MB90210 Series

• PWC data buffer register (PWCR)

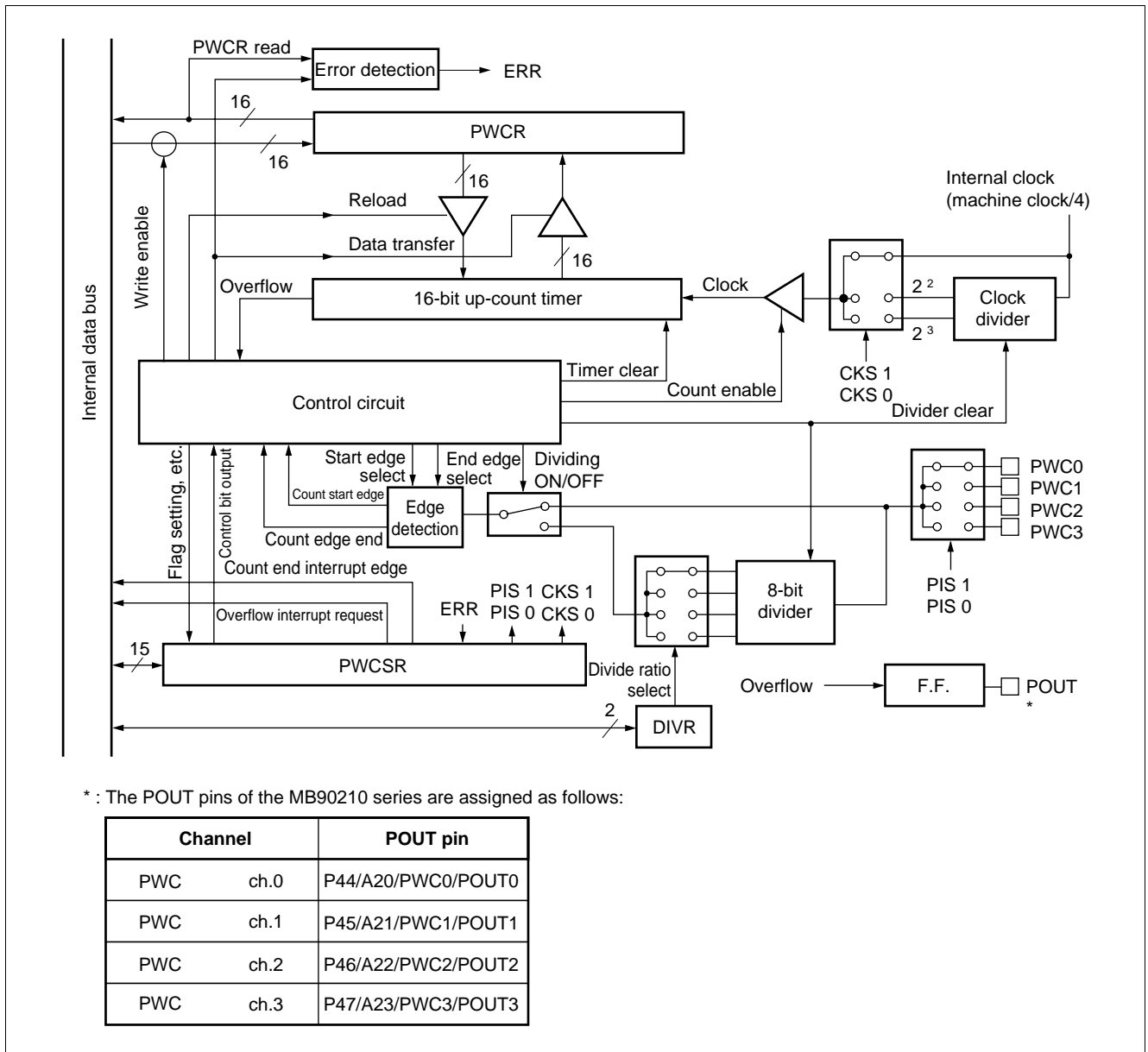


• PWC divide ratio control register (DIVR)



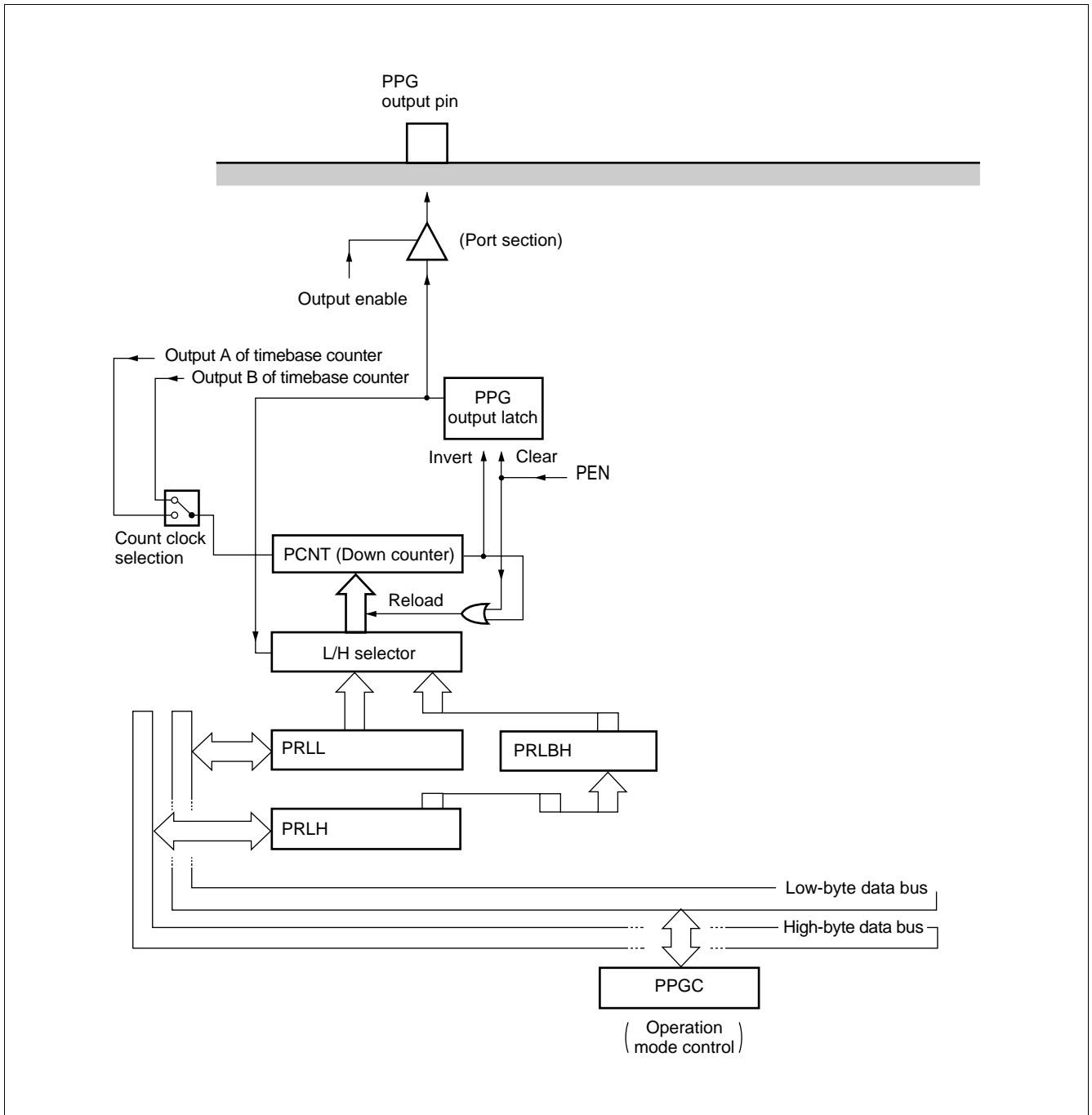
MB90210 Series

(2) Block Diagram

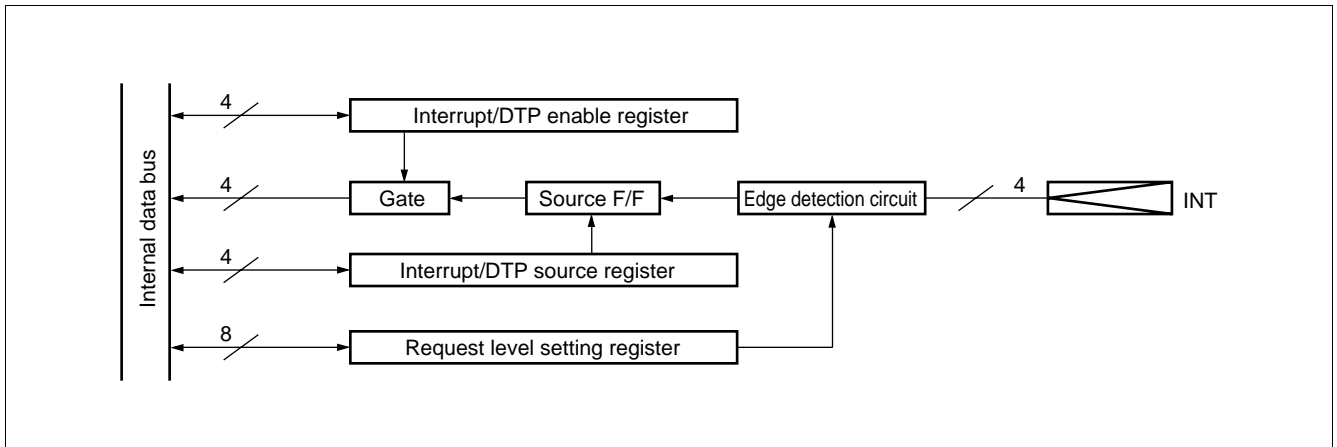


MB90210 Series

(2) Block Diagram



(2) Block Diagram



MB90210 Series

9. Watchdog Timer and Timebase Timer

The watchdog timer consists of a 2-bit watchdog counter using carry signals from an 18-bit timebase timer as the clock source, a control register, and a watchdog reset control section. The timebase timer consists of an 18-bit timer and an interval interrupt control circuit.

(1) Register Configuration

• Watchdog timer control register (WTC)

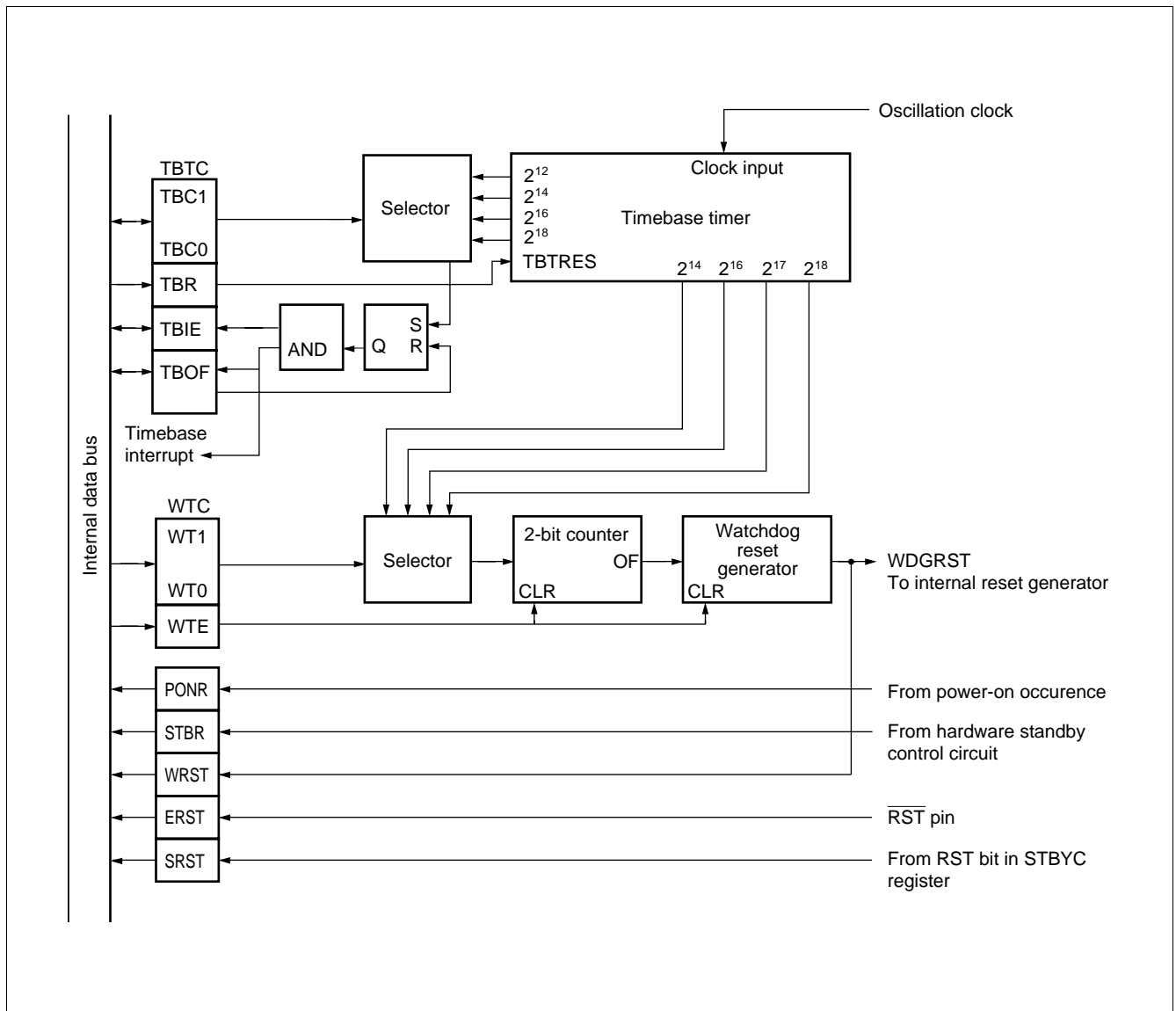
| Watchdog timer control register | | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------------------------|---------------------|-----|------|------|------|------|------|-----|-----|-----|-----|
| Address: | 0000A8 _H | | PONR | STBR | WRST | ERST | SRST | WTE | WT1 | WT0 | WTC |
| Read/write | → | | (R) | (R) | (R) | (R) | (R) | (W) | (W) | (W) | |
| Initial value | → | | (X) | (X) | (X) | (X) | (X) | (X) | (X) | (X) | |

• Timebase timer control register (TBTC)

| Timebase timer control register | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---------------------------------|---------------------|-----|----------|-----|-----|-------|-------|-----|-------|-------|------|
| Address: | 0000A9 _H | | Reserved | — | — | TBIE | TBOF | TBR | TBC1 | TBC0 | TBTC |
| Read/write | → | | (W) | (—) | (—) | (R/W) | (R/W) | (R) | (R/W) | (R/W) | |
| Initial value | → | | (1) | (—) | (—) | (0) | (0) | (0) | (0) | (0) | |

MB90210 Series

(2) Block Diagram



MB90210 Series

10. Delayed Interrupt Generation Module

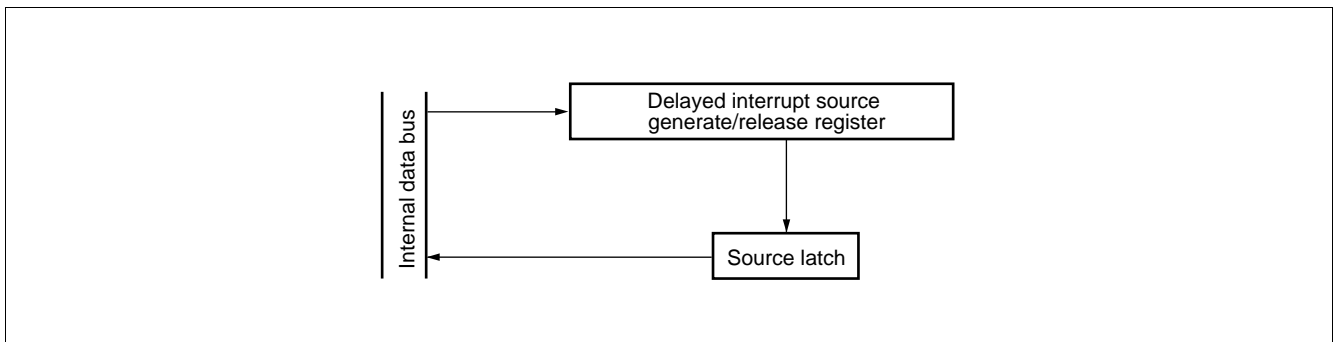
The delayed interrupt generation module is used to generate an interrupt for task switching. Using this module allows an interrupt request to the F²MC-16F CPU to generate or cancel by software.

(1) Register Configuration

- Delayed interrupt source generate/release register (DIRR)

| Delayed interrupt source generate/release register | | Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|--|---------|-----|-----|-----|-----|-----|-----|-----|-----|-------|------|
| Address: | 00009FH | | — | — | — | — | — | — | — | R0 | DIRR |
| Read/write | → | (—) | (—) | (—) | (—) | (—) | (—) | (—) | (—) | (R/W) | |
| Initial value | → | (—) | (—) | (—) | (—) | (—) | (—) | (—) | (—) | (0) | |

(2) Block Diagram



11. Write-inhibit RAM

The write-inhibit RAM is write-protectable with the \overline{WI} pin input. Maintaining the “L” level input to the \overline{WI} pin prevents a certain area of RAM from being written. The \overline{WI} pin has a 4-machine-cycle filter.

(1) Register Configuration

- WI control register (WICR)

| WI control register | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------------|---------------------|-----|-----|-----|-------|-----|-----|-----|-----|------|
| Address: | 00008E _H | — | — | — | WI | — | — | — | — | WICR |
| Read/write | → | (—) | (—) | (—) | (R/W) | (—) | (—) | (—) | (—) | |
| Initial value | → | (—) | (—) | (—) | (1) | (—) | (—) | (—) | (—) | |

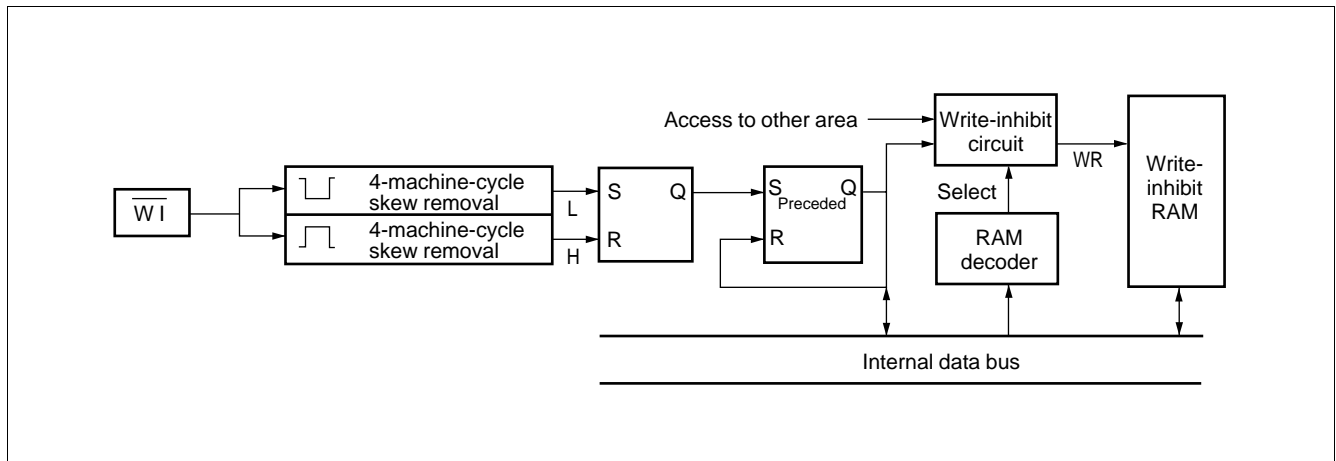
(2) Write-inhibit RAM Area

Write-inhibit RAM area

001100_H to 0011FF_H (MB90214/P214A/P214B/W214A/W214B)

001100_H to 0012FF_H (MB90V210)

(3) Block Diagram



MB90210 Series

12. Low-power Consumption Modes, Oscillation Stabilization Delay Time, and Gear Function

The MB90210 series has three low-power consumption modes: the sleep mode, the stop mode, the hardware standby mode, and gear function.

Sleep mode is used to suspend only the CPU operation clock; the other components remain in operation. Stop mode and hardware standby mode stop oscillation, minimizing the power consumption while holding data.

The clock gear function divides the external clock frequency, which is used usually as it is, to provide a lower machine clock frequency. This function can therefore lower the overall operation speed without changing the oscillation frequency. The function can select the machine clock as a division of the frequency of crystal oscillation or external clock input by 1, 2, 4, or 16.

The OSC1 and OSC0 bits can be used to set the oscillation stabilization delay time for wake-up from stop mode or hardware standby mode.

(1) Register Configuration

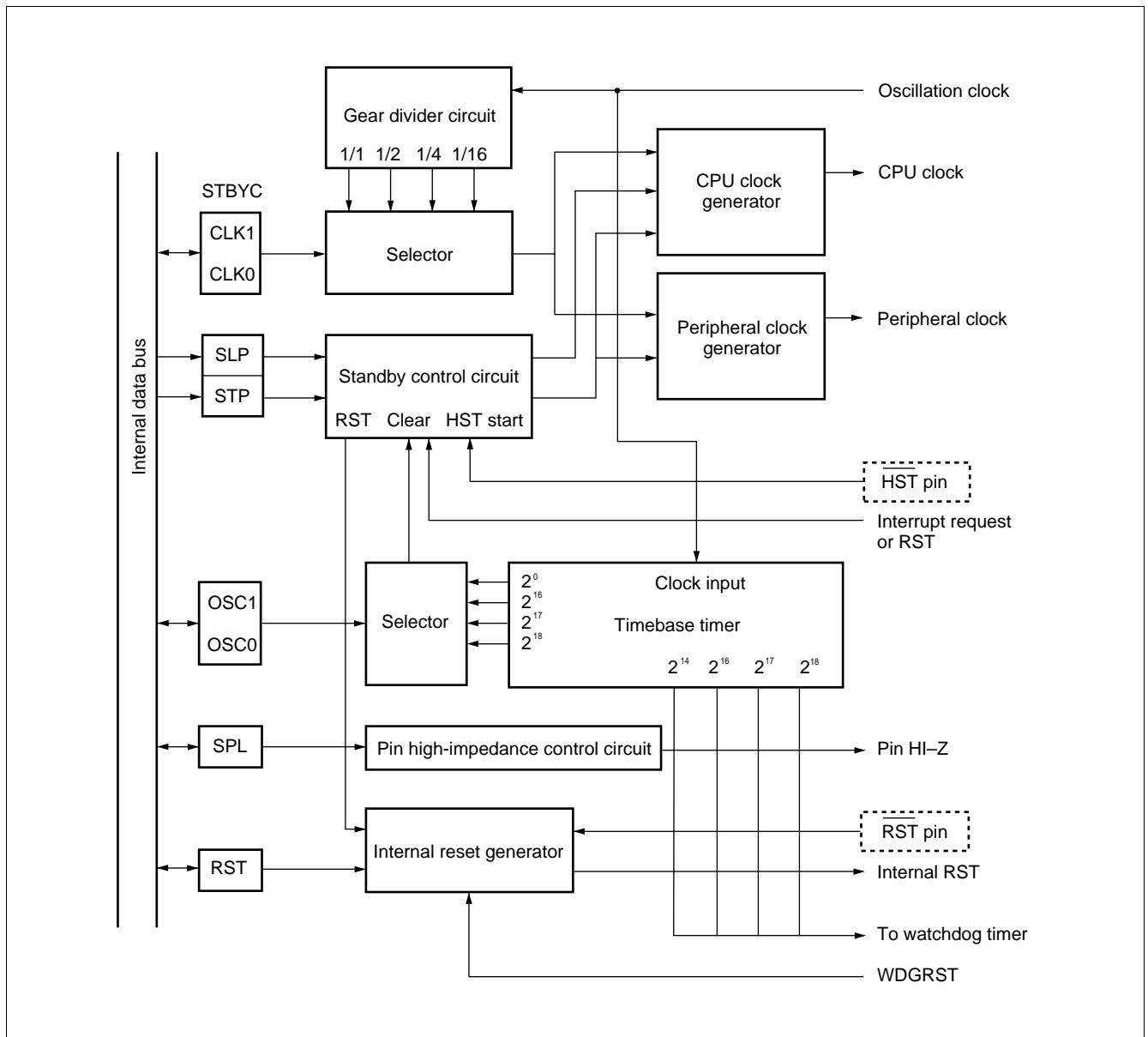
- Standby control register (STBYC)

| Standby control register | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|--------------------------|-----|-----|-----|-------|-------|-------|-------|-------|-------|-------|
| Address: 0000A0H | | STP | SLP | SPL | RST | OSC1 | OSC0 | CLK1 | CLK0 | STBYC |
| Read/write | → | (W) | (W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | (R/W) | |
| Initial value | → | (0) | (0) | (0) | (1) | (*) | (*) | (*) | (*) | |

Note: The initial value(*) of bit0 to bit3 is changed by reset source.

MB90210 Series

(2) Block Diagram



MB90210 Series

■ ELECTRICAL CHARACTERISTICS (MB90V210, device used for evaluation, is excluded)

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|--------------------------------|-----------------|--------------|----------------|----------------|------|--|
| | | | Min. | Max. | | |
| Power supply voltage | V_{CC} | V_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | |
| Program voltage | V_{PP} | V_{PP} | $V_{SS} - 0.3$ | 13.0 | V | MB90P214A/W214A MB90P214B/W214B |
| Analog power supply voltage | AV_{CC} | AV_{CC} | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | Power supply voltage for A/D converter |
| | AVRH AVRL | AVRH AVRL | $V_{SS} - 0.3$ | AV_{CC} | V | Reference voltage for A/D converter |
| Input voltage | V_I^{*1} | — | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| Output voltage | V_O | *2 | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| “L” level output current | I_{OL} | *3 | — | 20 | mA | Rush current |
| “L” level total output current | ΣI_{OL} | *3 | — | 50 | mA | Total output current |
| “H” level output current | I_{OH} | *2 | — | -10 | mA | Rush current |
| “H” level total output current | ΣI_{OH} | *2 | — | -48 | mA | Total output current |
| Power consumption | P_d | — | — | 650 | mW | |
| Operating temperature | T_A | — | -40 | +105 | °C | MB90214/P214B/W214B |
| | | | -40 | +85 | °C | MB90P214A/W214A |
| Storage temperature | T_{stg} | — | -55 | +150 | °C | |

*1: V_I and V_O must not exceed $V_{CC} + 0.3\text{ V}$.

*2: Output pins

P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P75, P80 to P82

*3: Output pins

P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P75, P80 to P82

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB90210 Series

2. Recommended Operating Conditions

(V_{ss} = AV_{ss} = 0.0 V)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|-----------------------------|------------------|------------------|------------------|-----------------------|------|---|
| | | | Min. | Max. | | |
| Power supply voltage | V _{cc} | V _{cc} | 4.5 | 5.5 | V | When operating |
| | | | 3.0 | 5.5 | V | Retains the RAM state in stop mode |
| Analog power supply voltage | AV _{cc} | AV _{cc} | 4.5 | V _{cc} + 0.3 | V | Power supply voltage for A/D converter |
| | AVRH | AVRH | AVRL | AV _{cc} | V | Reference voltage for A/D converter |
| | AVRL | AVRL | AV _{ss} | AVRH | V | |
| Clock frequency | F _c | — | 10 | 16 | MHz | |
| Operating temperature | T _A * | — | -40 | +105 | °C | Single-chip mode MB90214/P214B/W214B |
| | | | -40 | +85 | °C | Single-chip mode MB90P214A/W214A |
| | | | -40 | +70 | °C | External bus mode |

* : Excluding the temperature rise due to the heat produced.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

MB90210 Series

3. DC Characteristics

Single-chip mode MB90214/P214B/W214B : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P214A/W214A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)
 External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-----------------------------|------------|-------------|--|----------------|------|----------------|---------------|---|
| | | | | Min. | Typ. | Max. | | |
| “H” level input voltage | V_{IH} | *1 | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | CMOS level input |
| | V_{IHS} | *2 | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | Hysteresis input |
| | V_{IHM} | MD0 to MD2 | — | $V_{CC} - 0.3$ | — | $V_{CC} + 0.3$ | V | |
| “L” level input voltage | V_{IL} | *1 | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | CMOS level input |
| | V_{ILS} | *2 | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | Hysteresis input |
| | V_{ILM} | MD0 to MD2 | — | $V_{SS} - 0.3$ | — | $V_{SS} + 0.3$ | V | |
| “H” level output voltage | V_{OH} | *3 | $V_{CC} = 4.5\text{ V}$ $I_{OH} = -4.0\text{ mA}$ | $V_{CC} - 0.5$ | — | V_{CC} | V | |
| | V_{OH1} | X1 | $V_{CC} = 4.5\text{ V}$ $I_{OH} = -2.0\text{ mA}$ | $V_{CC} - 2.3$ | — | V_{CC} | V | |
| “L” level output voltage | V_{OL} | *4 | $V_{CC} = 4.5\text{ V}$ $I_{OL} = 4.0\text{ mA}$ | 0 | — | 0.4 | V | |
| | V_{OL1} | X1 | $V_{CC} = 4.5\text{ V}$ $I_{OL} = 2.0\text{ mA}$ | 0 | — | $V_{CC} - 2.3$ | V | |
| Input leakage current | I_I | *1 *2 | $V_{CC} = 5.5\text{ V}$ $0.2 V_{CC} < V_I < 0.8 V_{CC}$ | — | — | ± 10 | μA | Except pins with pull-up/pull-down resistor and RST pin |
| | I_{I2} | X0 | $V_{CC} = 5.5\text{ V}$ $0.2 V_{CC} < V_I < 0.8 V_{CC}$ | — | — | ± 25 | μA | |
| Analog power supply voltage | I_A | | $F_C = 16\text{ MHz}$ | — | 3 | 7 | mA | |
| | I_{AH} | AV_{CC} | — | — | — | 5^{*5} | μA | In stop mode, $T_A = +25^\circ\text{C}$ |
| Input capacitance | C_{IN} | *6 | — | — | 10 | — | pF | |
| Pull-up resistor | R_{pUlU} | RST | — | 22 | 50 | 110 | k Ω | ^{*7} MB90214 MB90P214A/ W214A/P214B/ W214B |
| | | MD1 | — | 110 | 300 | 650 | k Ω | ^{*7} MB90214 |
| | | Generic pin | — | 22 | 50 | 110 | k Ω | ^{*7} MB90214 |
| Pull-down resistor | R_{pUlD} | MD0, MD2 | — | 110 | 300 | 650 | k Ω | ^{*7} MB90214 |
| | | Generic pin | — | 22 | 50 | 110 | k Ω | ^{*7} MB90214 |

(Continued)

MB90210 Series

(Continued)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|------------------------|------------------|-----------------|-------------------------|-------|------|------|------|--|
| | | | | Min. | Typ. | Max. | | |
| Power supply voltage*9 | I _{CC} | V _{CC} | F _C = 16 MHz | — | 50*8 | 80 | mA | MB90214 |
| | | | | — | 70*8 | 100 | mA | MB90P214A/ W214A MB90P214B/ W214B |
| | I _{CCS} | V _{CC} | F _C = 16 MHz | — | — | 40 | mA | In sleep mode |
| | I _{CCH} | V _{CC} | — | — | 5 | 10 | μA | T _A = +25°C In stop mode In hardware standby input time |

*1: CMOS level input (P00 to P07, P10 to P17, X0)

*2: Hysteresis input pins (RST, HST, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P75, P80 to P82)

*3: Output pins (P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P75, P80 to P82)

*4: Output pins (P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P75, P80 to P82)

*5: The current value applies to the CPU stop mode with A/D converter inactive (V_{CC} = AV_{CC} = AVRH = +5.5 V).*6: Other than V_{CC}, V_{SS}, AV_{CC} and AV_{SS}

*7: A list of availabilities of pull-up/pull-down resistors

| Pin name | MB90214 | MB90P214A/W214A | MB90P214B/W214B |
|-------------|--|-----------------------------|-----------------------------|
| RST | Availability of pull-up resistors is optionally defined. | Pull-up resistors available | Pull-up resistors available |
| MD1 | Pull-up resistors available | Unavailable | Unavailable |
| MD0, MD2 | Pull-down resistors available | Unavailable | Unavailable |
| Generic pin | Availability of pull-up/pull-down resistors is optionally defined. | Unavailable | Unavailable |

*8: V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = +25°C, F_C = 16 MHz*9: Measurement condition of power supply current; external clock pin and output pin are open.
Measurement condition of V_{CC}; see the table above mentioned.

MB90210 Series

2. AC Characteristics

(1) Clock Timing Standards

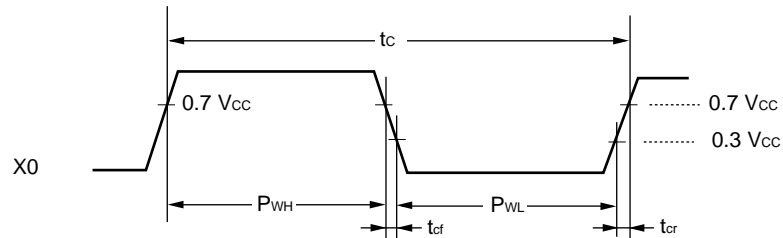
Single-chip mode MB90214/P214B/W214B : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)

MB90P214A/W214A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

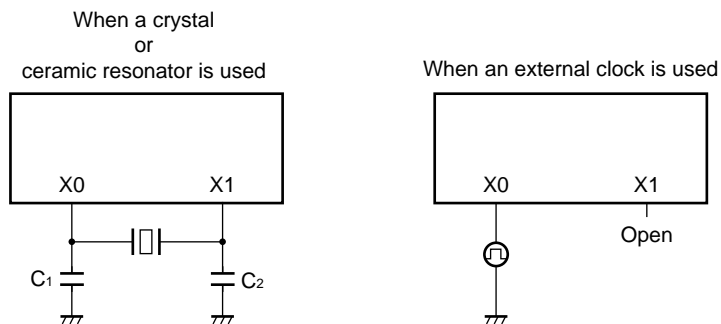
External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---------------------------------|----------------------|----------|-----------|-----------|------|-----------|------|-------------------|
| | | | | Min. | Typ. | Max. | | |
| Clock frequency | F_c | X0, X1 | — | 10 | — | 16 | MHz | |
| Clock cycle time | t_c | X0, X1 | — | 62.5 | — | 100 | ns | $1/F_c$ |
| Input clock pulse width | P_{WH} P_{WL} | X0 | — | $0.4 t_c$ | — | $0.6 t_c$ | ns | Duty ratio: 60% |
| Input clock rising/falling time | t_{cr} t_{cf} | X0 | — | — | — | 8 | ns | $t_{cr} + t_{cf}$ |

• Clock Input Timings



• Clock Conditions

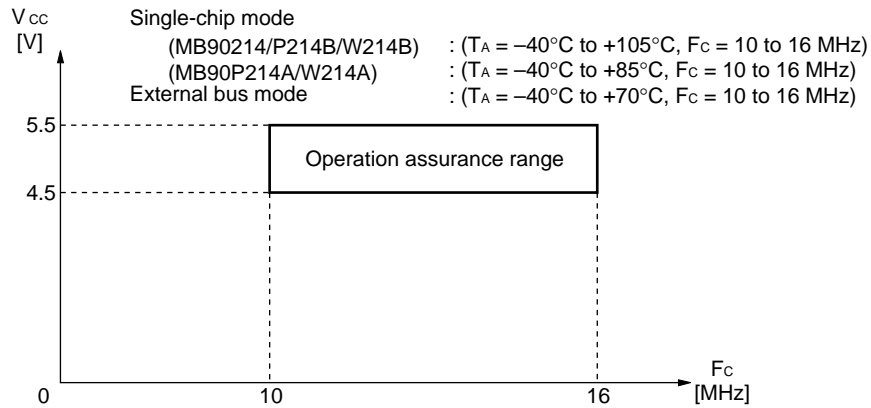


$C_1 = C_2 = 10\text{ pF}$

Select the optimum capacity value for the resonator.

MB90210 Series

• Relationship between Clock Frequency and Power Supply Voltage

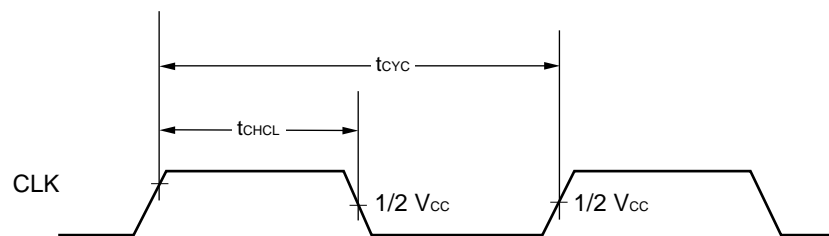


(2) Clock Output Timing Standards

External mode: ($V_{CC} = +4.5$ to $+5.5$ V, $V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|------------|----------|--------------------------|------------------|------|-------------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| Machine cycle time | t_{CYC} | CLK | Load condition: 80 pF | 62.5 | — | 1600 | ns | * |
| CLK $\uparrow \rightarrow$ CLK \downarrow | t_{CHCL} | | | $t_{CYC}/2 - 20$ | — | $t_{CYC}/2$ | ns | |

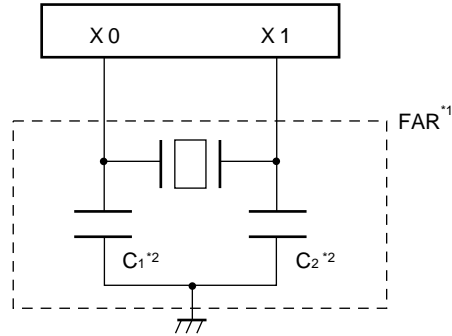
* : $t_{CYC} = n/F_c$, n gear ratio (1, 2, 4, 16)



MB90210 Series

(3) Recommended Resonator Manufacturers

• Sample Application of Piezoelectric Resonator (FAR Series)



*1: Fujitsu Acoustic Resonator

| FAR part number (built-in capacitor type) | Frequency | Initial deviation of FAR frequency ($T_A = +25^\circ\text{C}$) | Temperature characteristics of FAR frequency ($T_A = -20^\circ\text{C}$ to $+60^\circ\text{C}$) | Load capacitance*2 |
|--|-----------|--|--|-----------------------|
| FAR-C4C F-1 6000-□02 | 16.00 | $\pm 0.5\%$ | $\pm 0.5\%$ | Built-in |
| FAR-C4C F-1 6000-□12 | | $\pm 0.5\%$ | $\pm 0.5\%$ | |

Inquiry: FUJITSU LIMITED

(4) Reset and Hardware Standby Input Standards

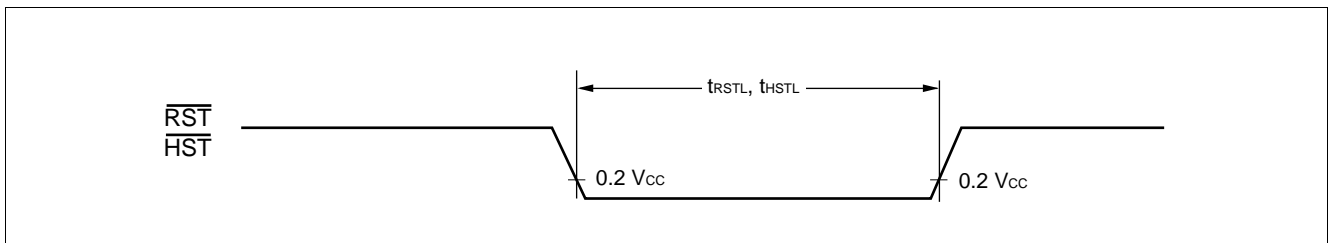
Single-chip mode MB90214/P214B/W214B : ($V_{CC} = +4.5\text{ V}$ to $+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$)

MB90P214A/W214A : ($V_{CC} = +4.5\text{ V}$ to $+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

External bus mode : ($V_{CC} = +4.5\text{ V}$ to $+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-----------------------------|------------|----------|-----------|-------------|------|------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| Reset input time | t_{RSTL} | RST | — | $5 t_{CYC}$ | — | — | ns | |
| Hardware standby input time | t_{HSTL} | HST | | $5 t_{CYC}$ | — | — | ns | * |

* : The machine cycle (t_{CYC}) at hardware standby input is set to 1/16 divided oscillation.



MB90210 Series

(5) Power on Supply Specifications (Power-on Reset)

Single-chip mode MB90214/P214B/W214B : ($V_{CC} = +4.5 \text{ V to } +5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C}$)

MB90P214A/W214A : ($V_{CC} = +4.5 \text{ V to } +5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

External bus mode : ($V_{CC} = +4.5 \text{ V to } +5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +70^\circ\text{C}$)

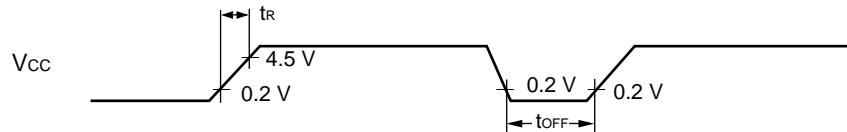
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---------------------------|-----------|----------|-----------|-------|------|------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| Power supply rising time | t_r | V_{CC} | — | — | — | 30 | ms | * |
| Power supply cut-off time | t_{OFF} | V_{CC} | — | 1 | — | — | ms | |

* : Before the power rising, V_{CC} must be less than $+0.2 \text{ V}$.

Notes: • The above specifications are for the power-on reset.

- Always apply power-on reset using these specifications, regardless of whether or not the power-on reset is needed.
- There are some internal registers (such as STBYC) which are only initialized by the power-on reset.

• Power-on Reset

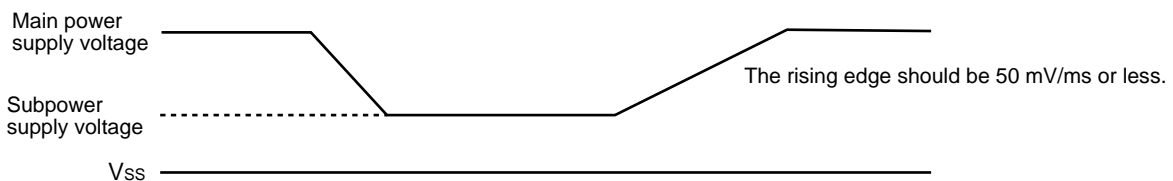


Note: Caution on switching power supply

Abrupt change of supply voltage may initiate power-on reset, even if the above requirements are not met.

It is, therefore, recommended to power up gradually during the instantaneous change of power supply as shown in the figure below.

• Changing Power Supply

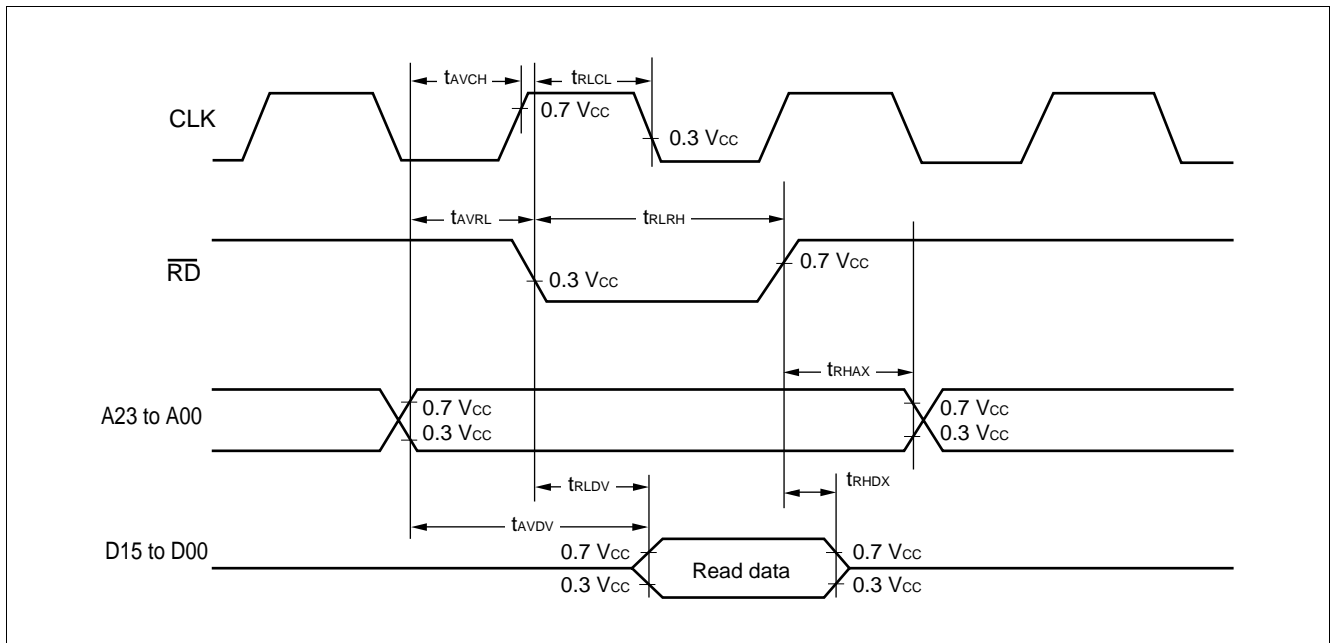


MB90210 Series

(6) Bus Read Timing

($V_{CC} = +4.5$ to $+5.5$, $V_{SS} = 0.0$ V, $T_A = -40^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|--|-------------------|------------------------------|--------------------------|-------------------------|---------------------------|------|---------|
| | | | | Min. | Max. | | |
| Valid address $\rightarrow \overline{\text{RD}} \downarrow$ time | t_{AVRL} | A23 to A00 | Load condition: 80 pF | $t_{\text{CYC}}/2 - 20$ | — | ns | |
| $\overline{\text{RD}}$ pulse width | t_{RLRH} | RD | | $t_{\text{CYC}} - 25$ | — | ns | |
| $\overline{\text{RD}} \downarrow \rightarrow$ valid data input | t_{RLDV} | D15 to D00 | | — | $t_{\text{CYC}} - 30$ | ns | |
| $\overline{\text{RD}} \uparrow \rightarrow$ data hold time | t_{RHDX} | | | 0 | — | ns | |
| Valid address \rightarrow valid data input | t_{AVDV} | | | — | $3 t_{\text{CYC}}/2 - 40$ | ns | |
| $\overline{\text{RD}} \uparrow \rightarrow$ address valid time | t_{RHAX} | A23 to A00 | | $t_{\text{CYC}}/2 - 20$ | — | ns | |
| Valid address $\rightarrow \text{CLK} \uparrow$ time | t_{AVCH} | A23 to A00 CLK | | $t_{\text{CYC}}/2 - 25$ | — | ns | |
| $\overline{\text{RD}} \downarrow \rightarrow \text{CLK} \downarrow$ time | t_{RLCL} | $\overline{\text{RD}}$, CLK | | $t_{\text{CYC}}/2 - 25$ | — | ns | |

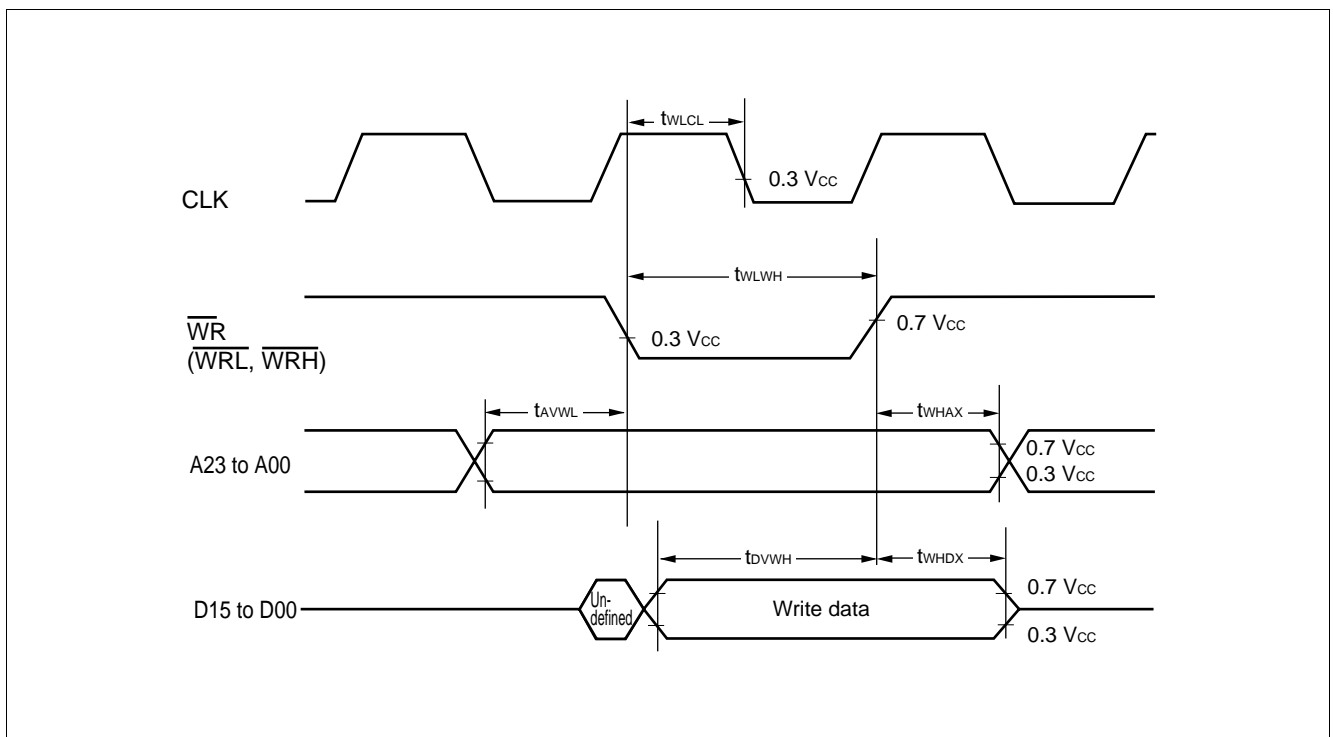


MB90210 Series

(7) Bus Write Timing

($V_{CC} = +4.5$ to $+5.5$ V, $V_{SS} = 0.0$ V, $T_A = -40^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|--|------------|---|--------------------------|------------------|------|------|---------|
| | | | | Min. | Max. | | |
| Valid address $\rightarrow \overline{WR} \downarrow$ time | t_{AVWL} | A23 to A00 | Load condition: 80 pF | $t_{CYC}/2 - 20$ | — | ns | |
| $\overline{WR} \downarrow$ pulse width | t_{WLWH} | \overline{WRL} , \overline{WRH} | | $t_{CYC} - 25$ | — | ns | |
| Valid data output $\rightarrow \overline{WR} \uparrow$ time | t_{DVWH} | D15 to D00 | | $t_{CYC} - 40$ | — | ns | |
| $\overline{WR} \uparrow \rightarrow$ data hold time | t_{WHDX} | | | $t_{CYC}/2 - 20$ | — | ns | |
| $\overline{WR} \uparrow \rightarrow$ address valid time | t_{WHAX} | A23 to A00 | | $t_{CYC}/2 - 20$ | — | ns | |
| $\overline{WR} \downarrow \rightarrow$ CLK \downarrow time | t_{WLCH} | \overline{WRL} , \overline{WRH} , CLK | | $t_{CYC}/2 - 25$ | — | ns | |



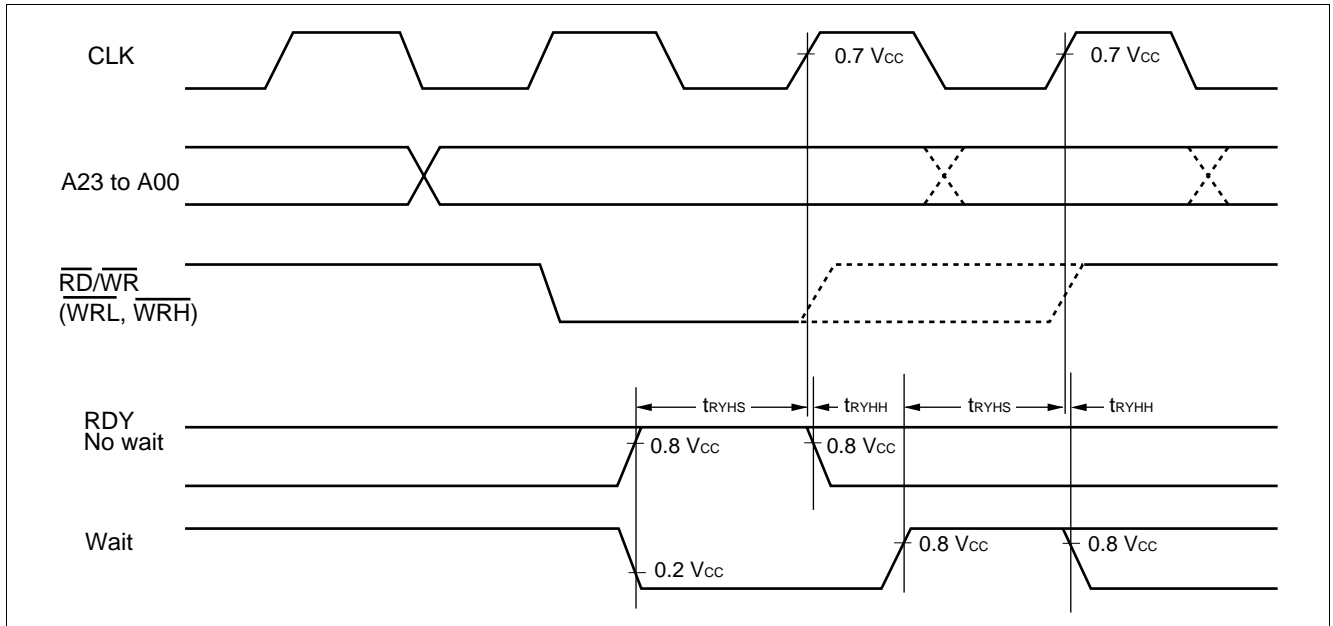
MB90210 Series

(8) Ready Signal Input Timing

($V_{CC} = +4.5$ to $+5.5$ V, $V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|----------------|------------|----------|--------------------------|-------|------|------|---------|
| | | | | Min. | Max. | | |
| RDY setup time | t_{RYHS} | RDY | Load condition: 80 pF | 40 | — | ns | |
| RDY hold time | t_{RYHH} | | | 0 | — | ns | |

Note: Use the auto-ready function if the RDY setup time is insufficient.

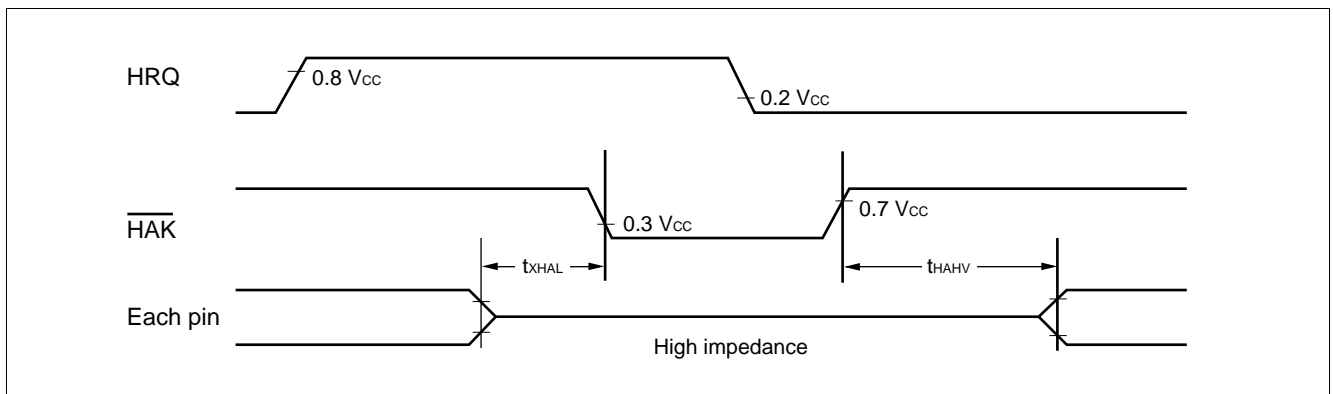


(9) Hold Timing

($V_{CC} = +4.5$ to $+5.5$ V, $V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|------------|------------------|--------------------------|-----------|------------|------|---------|
| | | | | Min. | Max. | | |
| Pin floating $\rightarrow \overline{HAK} \downarrow$ time | t_{XHAL} | \overline{HAK} | Load condition: 80 pF | 30 | t_{CYC} | ns | |
| $\overline{HAK} \uparrow \rightarrow$ pin valid time | t_{HAHV} | | | t_{CYC} | $2t_{CYC}$ | ns | |

Note: It takes at least one cycle for \overline{HAK} to vary after HRQ is fetched.



MB90210 Series

(10) UART Timing

Single-chip mode MB90214/P214B/W214B : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)

MB90P214A/W214A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

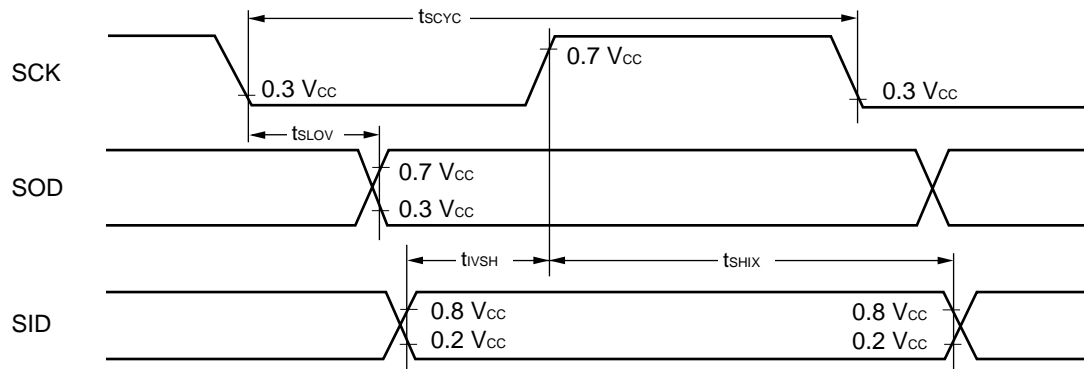
External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---------------------------------|-------------------|----------|--------------------------|--------------------|------|------|--|
| | | | | Min. | Max. | | |
| Serial clock cycle time | t _{SCYC} | — | Load condition: 80 pF | 8 t _{CYC} | — | ns | Internal shift clock mode output pin |
| SCLK ↓ → SOUT delay time | t _{SLOV} | | | -80 | 80 | ns | |
| Valid SIN → SCLK ↑ | t _{IVSH} | | | 100 | — | ns | |
| SCLK ↑ → Valid SIN hold time | t _{SHIX} | | | 60 | — | ns | |
| Serial clock "H" pulse width | t _{SHSL} | | | 4 t _{CYC} | — | ns | External shift clock mode output pin |
| Serial clock "L" pulse width | t _{SLSH} | | | 4 t _{CYC} | — | ns | |
| SCLK ↓ → SOUT delay time | t _{SLOV} | | | — | 150 | ns | |
| Valid SIN → SCLK ↑ | t _{IVSH} | | | 60 | — | ns | |
| SCLK ↑ → Valid SIN hold time | t _{SHIX} | 60 | — | ns | | | |

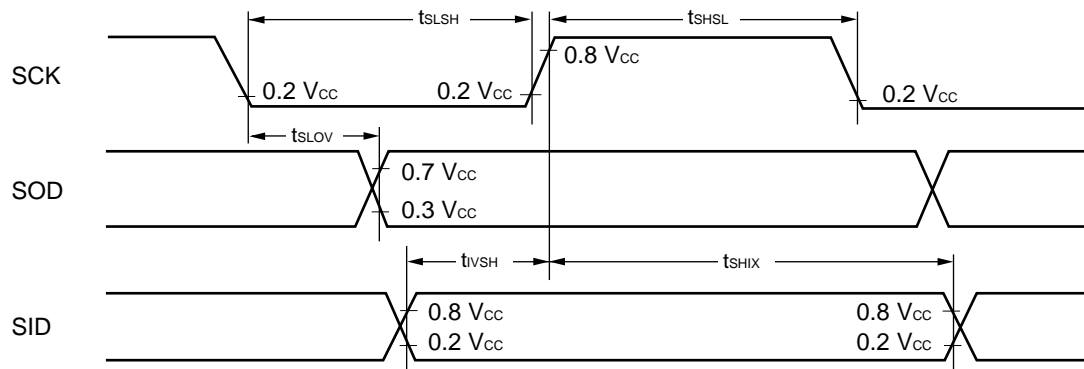
- Notes:
- These AC characteristics assume the CLK synchronous mode.
 - t_{CYC} is the machine cycle (unit: ns).

MB90210 Series

• Internal Shift Clock Mode



• External Shift Clock Mode

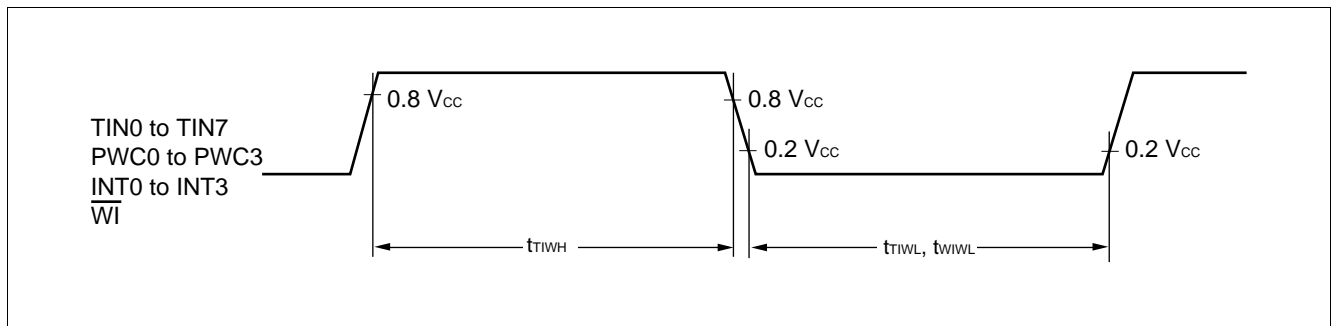


MB90210 Series

(11) Resource Input Timing

Single-chip mode MB90214/P214B/W214B : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P214A/W214A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)
 External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

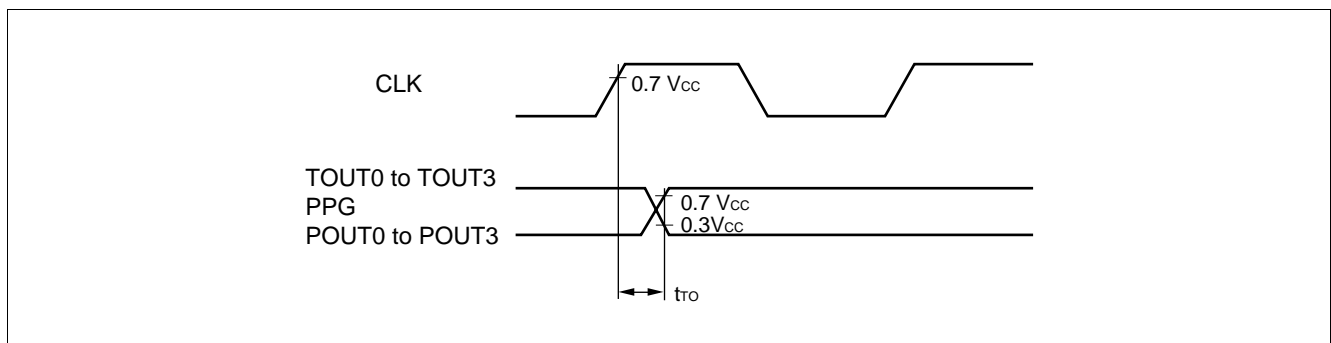
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-------------------|--------------------------|--------------|--------------------------|-------------|------|------|------|-----------------------------------|
| | | | | Min. | Typ. | Max. | | |
| Input pulse width | t_{TIWH} t_{TIWL} | TIN0 to TIN3 | Load condition: 80 pF | 4 t_{CYC} | — | — | ns | External event count input mode |
| | | | | 2 t_{CYC} | — | — | | Trigger input/ Gate input mode |
| | | TIN4 to TIN7 | | 2 t_{CYC} | — | — | ns | Gate input mode |
| | | PWC0 to PWC3 | | 2 t_{CYC} | — | — | ns | |
| | | INT0 to INT3 | | 3 t_{CYC} | — | — | ns | |
| | | ATG | | 2 t_{CYC} | — | — | ns | |
| | t_{WIWL} | WI | | 4 t_{CYC} | — | — | ns | |



(12) Resource Output Timing

Single-chip mode MB90214/P214B/W214B : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$)
 MB90P214A/W214A : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)
 External bus mode : ($V_{CC} = +4.5\text{ V to }+5.5\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+70^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|--|----------|---|--------------------------|-------|------|------|---------|
| | | | | Min. | Max. | | |
| CLK \uparrow \rightarrow TOUT transition time | t_{TO} | TOUT0 to TOUT3 PPG POUT0 to POUT3 | Load condition: 80 pF | — | 30 | ns | |



MB90210 Series

5. A/D Converter Electrical Characteristics

Single-chip mode MB90214/P214B/W214B:

($AV_{CC} = V_{CC} = +5.0 \pm 10\%$, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $+4.5$ V \cong $AV_{RH} - AV_{RL}$)

Single-chip mode MBP90214A/W214A:

($AV_{CC} = V_{CC} = +5.0 \pm 10\%$, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $+4.5$ V \cong $AV_{RH} - AV_{RL}$)

External bus mode:

($AV_{CC} = V_{CC} = +5.0 \pm 10\%$, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40^\circ\text{C}$ to $+70^\circ\text{C}$, $+4.5$ V \cong $AV_{RH} - AV_{RL}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|----------------------------------|------------|------------|---------------------|-----------------|-----------------|-----------------|---------------|-------------------|
| | | | | Min. | Typ. | Max. | | |
| Resolution | n | — | — | — | — | 10 | bit | |
| Total error | — | — | — | -3.0 | — | +3.0 | LSB | |
| Linearity error | — | — | — | -2.0 | — | +2.0 | LSB | |
| Differential linearity error | — | — | — | — | — | ± 1.5 | LSB | |
| Zero transition voltage | V_{OT} | AN0 to AN7 | — | $AV_{RL} - 1.5$ | $AV_{RL} + 0.5$ | $AV_{RL} + 2.5$ | LSB | |
| Full-scale transition voltage | V_{FST} | | — | $AV_{RH} - 3.5$ | $AV_{RH} - 1.5$ | $AV_{RH} + 0.5$ | LSB | |
| Conversion time | T_{CONV} | — | $t_{CYC} = 62.5$ ns | 6.125 | — | — | μs | 98 machine cycles |
| Sampling period | T_{SAMP} | — | | 3.75 | — | — | μs | 60 machine cycles |
| Analog port input current | I_{AIN} | AN0 to AN7 | — | — | — | ± 0.1 | μA | |
| Analog input voltage | V_{AIN} | | — | AV_{RL} | — | AV_{RH} | V | |
| Analog reference voltage | — | AVRH | — | AV_{RL} | — | AV_{CC} | V | |
| | | AVRL | — | AV_{SS} | — | AV_{RH} | V | |
| Reference voltage supply current | I_R | AVRH | — | — | 200 | 500 | μA | |
| | I_{RH} | | — | — | — | 5* | μA | |
| Interchannel disparity | — | AN0 to AN7 | — | — | — | 4 | LSB | |

* : The current value applies to the CPU stop mode with the A/D converter inactive ($V_{CC} = AV_{CC} = AV_{RH} = +5.5$ V).

Notes: (1) The smaller the $|AV_{RH} - AV_{RL}|$, the greater the error would become relatively.

(2) Use the output impedance of the external circuit for analog input under the following conditions:

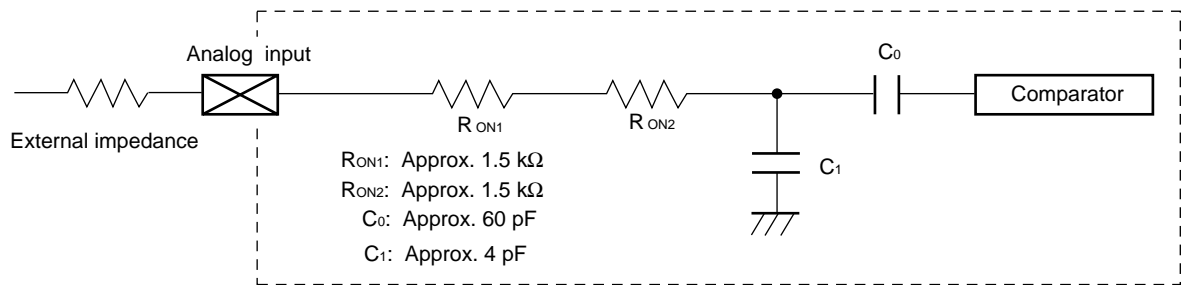
External circuit output impedance < approx. 10 k Ω (Sampling period \approx 3.75 μs , $t_{CYC} = 62.5$ ns)

(3) Precision values are standard values applicable to sleep mode.

(4) If V_{CC}/AV_{CC} or V_{SS}/AV_{SS} is caused by a noise to drop to below the analog input voltage, the analog input current is likely to increase. In such cases, a bypass capacitor or the like should be provided in the external circuit to suppress the noise.

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• Equivalent Circuit of Analog Input Circuit



Note: The values shown here are reference values.

6. A/D Converter Glossary

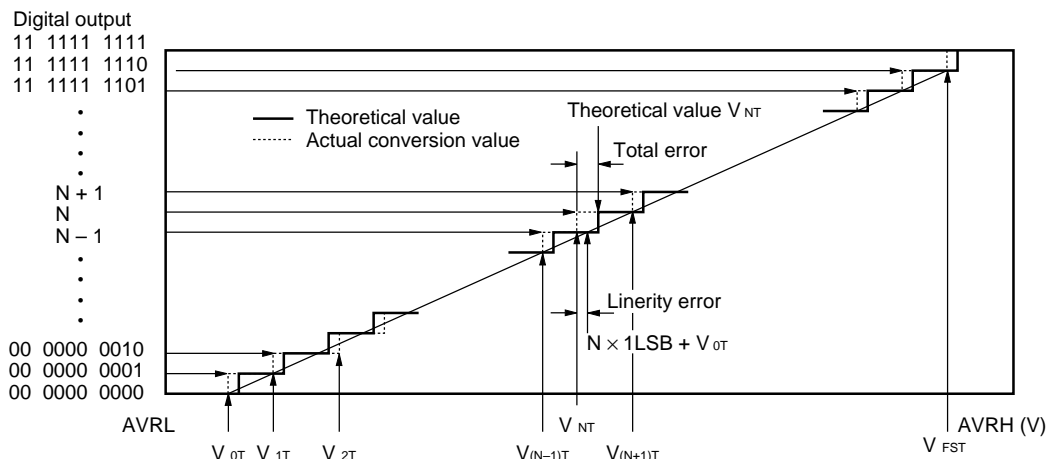
Resolution: Analog changes that are identifiable with the A/D converter

When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.

Total error: Difference between actual and logical values. This error is caused by a zero transition error, full-scale transition error, linearity error, differential linearity error, or by noise.

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.



$$\bullet \text{ 1LSB} = \frac{V_{FST} - V_{OT}}{1022} \cdot \text{1LSB theoretical value} = \frac{AV_{RH} - AV_{RL}}{1022}$$

$$\bullet \text{ Linearity error} = \frac{V_{NT} - (N \times \text{1LSB} + V_{OT})}{\text{1LSB}} \quad \left[\begin{array}{l} N = 0 \text{ to } 1022 \\ V_{NT} (N = 0) = V_{OT} \\ V_{NT} (N = 1022) = V_{FST} \end{array} \right.$$

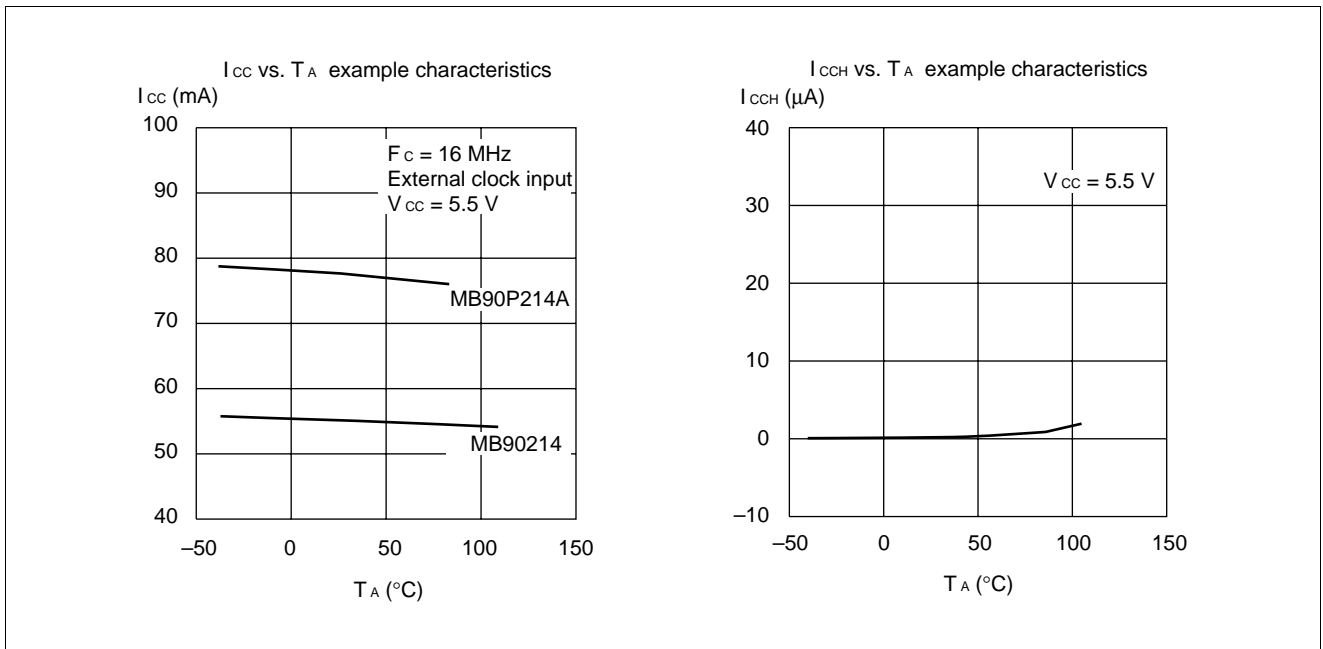
$$\bullet \text{ Differential linearity error} = \frac{V_{NT} - V_{(N-1)T}}{\text{1LSB}} - 1 \quad N = 1 \text{ to } 1022$$

$$\bullet \text{ Total error} = \frac{V_{NT} - \{ (N + 0.5) \times \text{1LSB theoretical value} \}}{\text{1LSB theoretical value}} \quad N = 0 \text{ to } 1022$$

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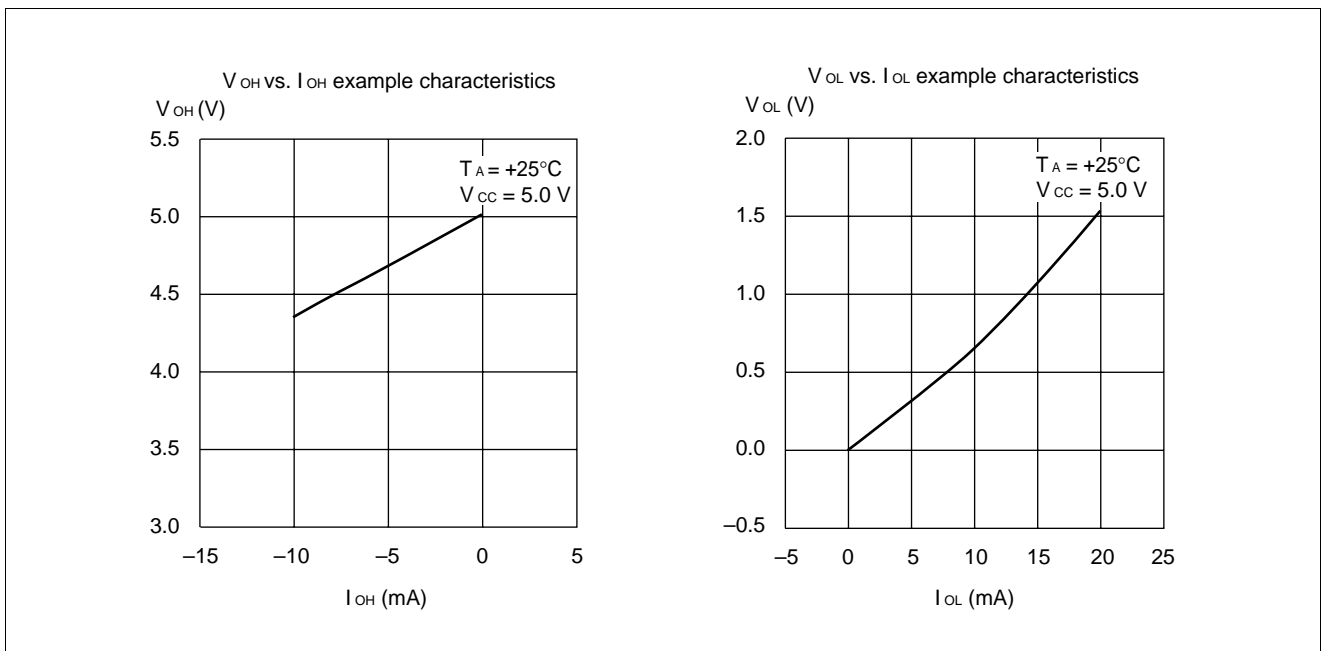
EXAMPLE CHARACTERISTICS

(1) Power Supply Current



Note: These are not assured value of characteristics but example characteristics.

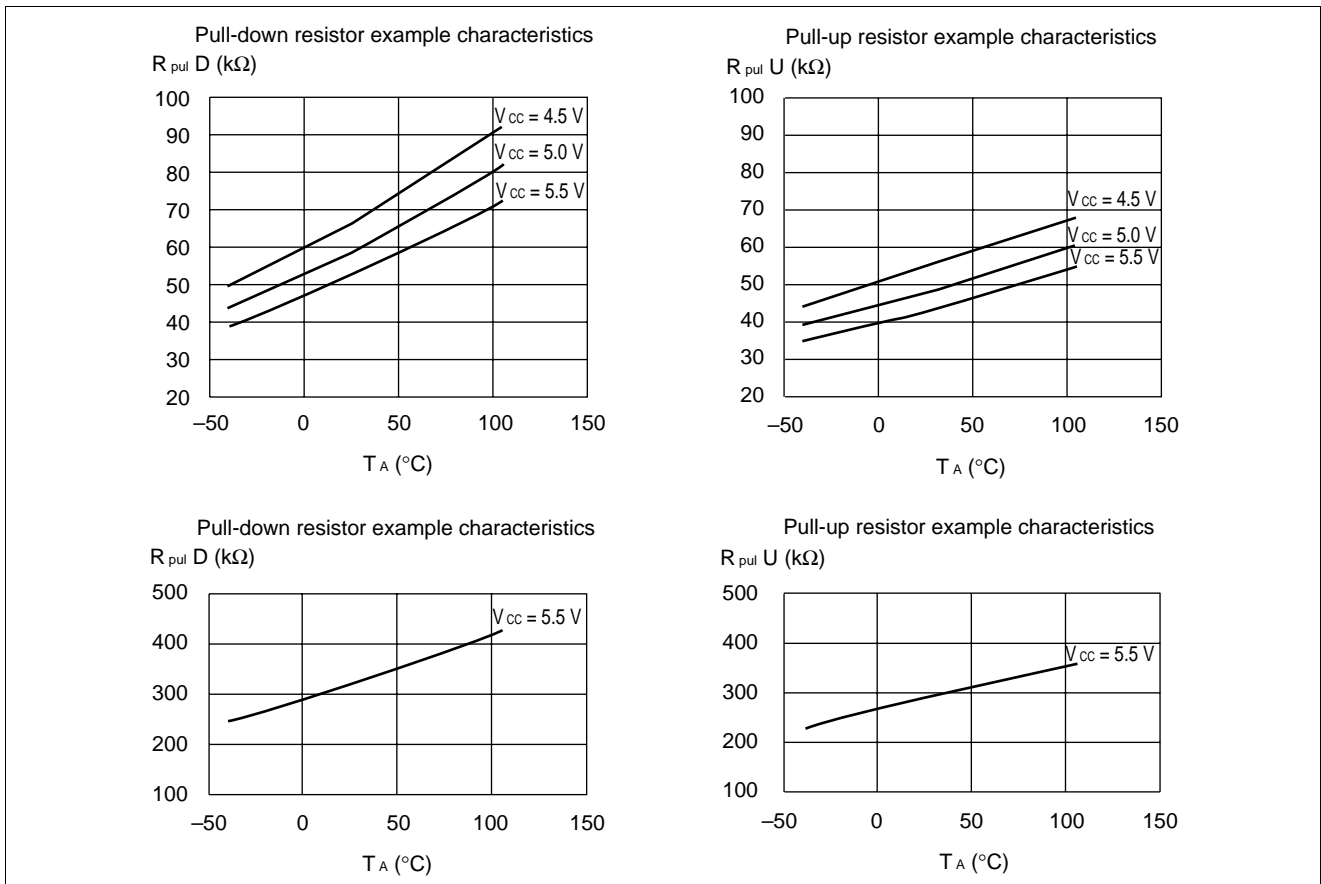
(2) Output Voltage



Note: These are not assured value of characteristics but example characteristics.

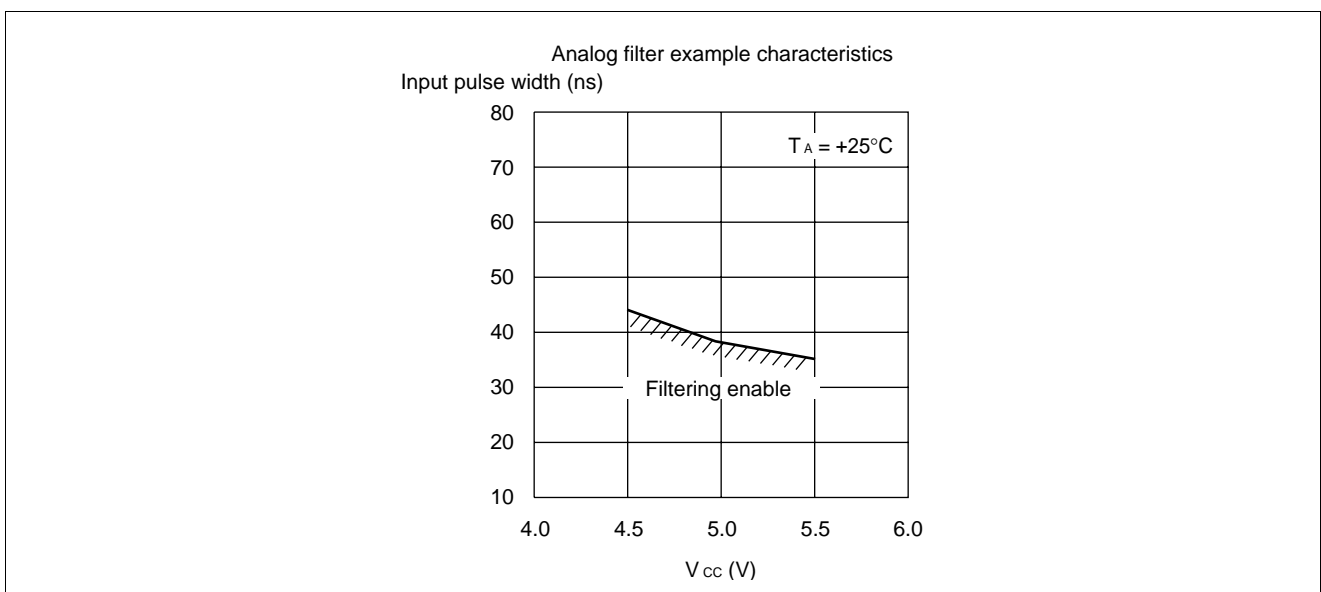
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(3) Pull-up/Pull-down Resistor



Note: These are not assured value of characteristics but example characteristics.

(4) Analog Filter



Note: These are not assured value of characteristics but example characteristics.

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■ INSTRUCTION SET (412 INSTRUCTIONS)

Table 1 Explanation of Items in Table of Instructions

| Item | Explanation |
|-----------|--|
| Mnemonic | Upper-case letters and symbols: Represented as they appear in assembler Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction. |
| # | Indicates the number of bytes. |
| ~ | Indicates the number of cycles. See Table 4 for details about meanings of letters in items. |
| B | Indicates the correction value for calculating the number of actual cycles during execution of instruction. The number of actual cycles during execution of instruction is summed with the value in the “cycles” column. |
| Operation | Indicates operation of instruction. |
| LH | Indicates special operations involving the bits 15 through 08 of the accumulator. Z: Transfers “0”. X: Extends before transferring. —: Transfers nothing. |
| AH | Indicates special operations involving the high-order 16 bits in the accumulator. *: Transfers from AL to AH. —: No transfer. Z: Transfers 00 _H to AH. X: Transfers 00 _H or FF _H to AH by extending AL. |
| I | Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). *: Changes due to execution of instruction. —: No change. S: Set by execution of instruction. R: Reset by execution of instruction. |
| S | |
| T | |
| N | |
| Z | |
| V | |
| C | |
| RMW | Indicates whether the instruction is a read-modify-write instruction (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory). *: Instruction is a read-modify-write instruction —: Instruction is not a read-modify-write instruction Note: Cannot be used for addresses that have different meanings depending on whether they are read or written. |

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Table 2 Explanation of Symbols in Table of Instructions

| Symbol | Explanation |
|-----------------|--|
| A | 32-bit accumulator The number of bits used varies according to the instruction. Byte: Low order 8 bits of AL Word: 16 bits of AL Long: 32 bits of AL, AH |
| AH | High-order 16 bits of A |
| AL | Low-order 16 bits of A |
| SP | Stack pointer (USP or SSP) |
| PC | Program counter |
| SPCU | Stack pointer upper limit register |
| SPCL | Stack pointer lower limit register |
| PCB | Program bank register |
| DTB | Data bank register |
| ADB | Additional data bank register |
| SSB | System stack bank register |
| USB | User stack bank register |
| SPB | Current stack bank register (SSB or USB) |
| DPR | Direct page register |
| brg1 | DTB, ADB, SSB, USB, DPR, PCB, SPB |
| brg2 | DTB, ADB, SSB, USB, DPR, SPB |
| Ri | R0, R1, R2, R3, R4, R5, R6, R7 |
| RWi | RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7 |
| RWj | RW0, RW1, RW2, RW3 |
| RLi | RL0, RL1, RL2, RL3 |
| dir | Compact direct addressing |
| addr16 | Direct addressing |
| addr24 | Physical direct addressing |
| addr24 0 to 15 | Bits 0 to 15 of addr24 |
| addr24 16 to 23 | Bits 16 to 23 of addr24 |
| io | I/O area (000000 _H to 0000FF _H) |

(Continued)

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(Continued)

| Symbol | Explanation |
|--|---|
| #imm4 #imm8 #imm16 #imm32 ext (imm8) | 4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data |
| disp8 disp16 | 8-bit displacement 16-bit displacement |
| bp | Bit offset value |
| vct4 vct8 | Vector number (0 to 15) Vector number (0 to 255) |
| ()b | Bit address |
| rel ear eam | Branch specification relative to PC Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F) |
| rlst | Register list |

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Table 3 Effective Address Fields

| Code | Notation | Address format | Number of bytes in address extension* |
|--|--|--|---------------------------------------|
| 00 01 02 03 04 05 06 07 | R0 RW0 RL0 R1 RW1 (RL0) R2 RW2 RL1 R3 RW3 (RL1) R4 RW4 RL2 R5 RW5 (RL2) R6 RW6 RL3 R7 RW7 (RL3) | Register direct "ea" corresponds to byte, word, and long-word types, starting from the left | — |
| 08 09 0A 0B | @RW0 @RW1 @RW2 @RW3 | Register indirect | 0 |
| 0C 0D 0E 0F | @RW0 + @RW1 + @RW2 + @RW3 + | Register indirect with post-increment | 0 |
| 10 11 12 13 14 15 16 17 | @RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8 | Register indirect with 8-bit displacement | 1 |
| 18 19 1A 1B | @RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16 | Register indirect with 16-bit displacement | 2 |
| 1C 1D 1E 1F | @RW0 + RW7 @RW1 + RW7 @PC + dip16 addr16 | Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address | 0 0 2 2 |

* : The number of bytes for address extension is indicated by the "+" symbol in the "#" (number of bytes) column in the Table of Instructions.

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Table 4 Number of Execution Cycles for Each Form of Addressing

| Code | Operand | (a)* |
|----------|------------------|--|
| | | Number of execution cycles for each form of addressing |
| 00 to 07 | Ri RWi RLi | Listed in Table of Instructions |
| 08 to 0B | @RWj | 1 |
| 0C to 0F | @RWj + | 4 |
| 10 to 17 | @RWi + disp8 | 1 |
| 18 to 1B | @RWj + disp16 | 1 |
| 1C | @RW0 + RW7 | 2 |
| 1D | @RW1 + RW7 | 2 |
| 1E | @PC + dip16 | 2 |
| 1F | @addr16 | 1 |

* :“(a)” is used in the “cycles” (number of cycles) column and column B (correction value) in the Table of Instructions.

Table 5 Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles

| Operand | (b)* | (c)* | (d)* |
|----------------------------------|------|------|------|
| | byte | word | long |
| Internal register | + 0 | + 0 | + 0 |
| Internal RAM even address | + 0 | + 0 | + 0 |
| Internal RAM odd address | + 0 | + 1 | + 2 |
| Even address not in internal RAM | + 1 | + 1 | + 2 |
| Odd address not in internal RAM | + 1 | + 3 | + 6 |
| External data bus (8 bits) | + 1 | + 3 | + 6 |

* :“(b)”, “(c)”, and “(d)” are used in the “cycles” (number of cycles) column and column B (correction value) in the Table of Instructions.

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Table 6 Transfer Instructions (Byte) [50 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|--------------------|----|--------|-----|----------------------------|----|----|---|---|---|---|---|---|---|-----|
| MOV A, dir | 2 | 2 | (b) | byte (A) ← (dir) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, addr16 | 3 | 2 | (b) | byte (A) ← (addr16) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, Ri | 1 | 1 | 0 | byte (A) ← (Ri) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, ear | 2 | 1 | 0 | byte (A) ← (ear) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, eam | 2+ | 2+ (a) | (b) | byte (A) ← (eam) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, io | 2 | 2 | (b) | byte (A) ← (io) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, #imm8 | 2 | 2 | 0 | byte (A) ← imm8 | Z | * | — | — | — | * | * | — | — | — |
| MOV A, @A | 2 | 2 | (b) | byte (A) ← ((A)) | Z | — | — | — | — | * | * | — | — | — |
| MOV A, @RLi+disp8 | 3 | 6 | (b) | byte (A) ← ((RLi))+disp8) | Z | * | — | — | — | * | * | — | — | — |
| MOV A, @SP+disp8 | 3 | 3 | (b) | byte (A) ← ((SP)+disp8) | Z | * | — | — | — | * | * | — | — | — |
| MOVP A, addr24 | 5 | 3 | (b) | byte (A) ← (addr24) | Z | * | — | — | — | * | * | — | — | — |
| MOVP A, @A | 2 | 2 | (b) | byte (A) ← ((A)) | Z | — | — | — | — | * | * | — | — | — |
| MOVN A, #imm4 | 1 | 1 | 0 | byte (A) ← imm4 | Z | * | — | — | — | R | * | — | — | — |
| MOVX A, dir | 2 | 2 | (b) | byte (A) ← (dir) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, addr16 | 3 | 2 | (b) | byte (A) ← (addr16) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, Ri | 2 | 1 | 0 | byte (A) ← (Ri) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, ear | 2 | 1 | 0 | byte (A) ← (ear) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, eam | 2+ | 2+ (a) | (b) | byte (A) ← (eam) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, io | 2 | 2 | (b) | byte (A) ← (io) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, #imm8 | 2 | 2 | 0 | byte (A) ← imm8 | X | * | — | — | — | * | * | — | — | — |
| MOVX A, @A | 2 | 2 | (b) | byte (A) ← ((A)) | X | — | — | — | — | * | * | — | — | — |
| MOVX A, @RWi+disp8 | 2 | 3 | (b) | byte (A) ← ((RWi))+disp8) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, @RLi+disp8 | 3 | 6 | (b) | byte (A) ← ((RLi))+disp8) | X | * | — | — | — | * | * | — | — | — |
| MOVX A, @SP+disp8 | 3 | 3 | (b) | byte (A) ← ((SP)+disp8) | X | * | — | — | — | * | * | — | — | — |
| MOVXPX A, addr24 | 5 | 3 | (b) | byte (A) ← (addr24) | X | * | — | — | — | * | * | — | — | — |
| MOVXPX A, @A | 2 | 2 | (b) | byte (A) ← ((A)) | X | — | — | — | — | * | * | — | — | — |
| MOV dir, A | 2 | 2 | (b) | byte (dir) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV addr16, A | 3 | 2 | (b) | byte (addr16) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV Ri, A | 1 | 1 | 0 | byte (Ri) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV ear, A | 2 | 2 | 0 | byte (ear) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV eam, A | 2+ | 2+ (a) | (b) | byte (eam) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV io, A | 2 | 2 | (b) | byte (io) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV @RLi+disp8, A | 3 | 6 | (b) | byte ((RLi) + disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV @SP+disp8, A | 3 | 3 | (b) | byte ((SP)+disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVP addr24, A | 5 | 3 | (b) | byte (addr24) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOV Ri, ear | 2 | 2 | 0 | byte (Ri) ← (ear) | — | — | — | — | — | * | * | — | — | — |
| MOV Ri, eam | 2+ | 3+ (a) | (b) | byte (Ri) ← (eam) | — | — | — | — | — | * | * | — | — | — |
| MOVP @A, Ri | 2 | 3 | (b) | byte ((A)) ← (Ri) | — | — | — | — | — | * | * | — | — | — |
| MOV ear, Ri | 2 | 3 | 0 | byte (ear) ← (Ri) | — | — | — | — | — | * | * | — | — | — |
| MOV eam, Ri | 2+ | 3+ (a) | (b) | byte (eam) ← (Ri) | — | — | — | — | — | * | * | — | — | — |
| MOV Ri, #imm8 | 2 | 2 | 0 | byte (Ri) ← imm8 | — | — | — | — | — | * | * | — | — | — |
| MOV io, #imm8 | 3 | 3 | (b) | byte (io) ← imm8 | — | — | — | — | — | — | — | — | — | — |
| MOV dir, #imm8 | 3 | 3 | (b) | byte (dir) ← imm8 | — | — | — | — | — | — | — | — | — | — |
| MOV ear, #imm8 | 3 | 2 | 0 | byte (ear) ← imm8 | — | — | — | — | — | * | * | — | — | — |
| MOV eam, #imm8 | 3+ | 2+ (a) | (b) | byte (eam) ← imm8 | — | — | — | — | — | — | — | — | — | — |
| MOV @AL, AH | 2 | 2 | (b) | byte ((A)) ← (AH) | — | — | — | — | — | * | * | — | — | — |

(Continued)

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(Continued)

| Mnemonic | | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|---------|----|--------|--------|-------------------|----|----|---|---|---|---|---|---|---|-----|
| XCH | A, ear | 2 | 3 | 0 | byte (A) ↔ (ear) | Z | – | – | – | – | – | – | – | – | – |
| XCH | A, eam | 2+ | 3+ (a) | 2× (b) | byte (A) ↔ (eam) | Z | – | – | – | – | – | – | – | – | – |
| XCH | Ri, ear | 2 | 4 | 0 | byte (Ri) ↔ (ear) | – | – | – | – | – | – | – | – | – | – |
| XCH | Ri, eam | 2+ | 5+ (a) | 2× (b) | byte (Ri) ↔ (eam) | – | – | – | – | – | – | – | – | – | – |

For an explanation of “(a)” and “(b)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 7 Transfer Instructions (Word) [40 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|--------------------|----|--------|--------|---------------------------|----|----|---|---|---|---|---|---|---|-----|
| MOVW A, dir | 2 | 2 | (c) | word (A) ← (dir) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, addr16 | 3 | 2 | (c) | word (A) ← (addr16) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, SP | 1 | 2 | 0 | word (A) ← (SP) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, RWi | 1 | 1 | 0 | word (A) ← (RWi) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, ear | 2 | 1 | 0 | word (A) ← (ear) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, eam | 2+ | 2+ (a) | (c) | word (A) ← (eam) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, io | 2 | 2 | (c) | word (A) ← (io) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @A | 2 | 2 | (c) | word (A) ← ((A)) | — | — | — | — | — | * | * | — | — | — |
| MOVW A, #imm16 | 3 | 2 | 0 | word (A) ← imm16 | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @RWi+disp8 | 2 | 3 | (c) | word (A) ← ((RWi) +disp8) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @RLi+disp8 | 3 | 6 | (c) | word (A) ← ((RLi) +disp8) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @SP+disp8 | 3 | 3 | (c) | word (A) ← ((SP) +disp8) | — | * | — | — | — | * | * | — | — | — |
| MOVW A, @A | 2 | 2 | (c) | word (A) ← ((A)) | — | — | — | — | — | * | * | — | — | — |
| MOVW dir, A | 2 | 2 | (c) | word (dir) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW addr16, A | 3 | 2 | (c) | word (addr16) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW SP, # imm16 | 4 | 2 | 0 | word (SP) ← imm16 | — | — | — | — | — | * | * | — | — | — |
| MOVW SP, A | 1 | 2 | 0 | word (SP) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW RWi, A | 1 | 1 | 0 | word (RWi) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW ear, A | 2 | 2 | 0 | word (ear) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW eam, A | 2+ | 2+ (a) | (c) | word (eam) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW io, A | 2 | 2 | (c) | word (io) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW @RWi+disp8, A | 2 | 3 | (c) | word ((RWi) +disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW @RLi+disp8, A | 3 | 6 | (c) | word ((RLi) +disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW @SP+disp8, A | 3 | 3 | (c) | word ((SP) +disp8) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW addr24, A | 5 | 3 | (c) | word (addr24) ← (A) | — | — | — | — | — | * | * | — | — | — |
| MOVW @A, RWi | 2 | 3 | (c) | word ((A)) ← (RWi) | — | — | — | — | — | * | * | — | — | — |
| MOVW RWi, ear | 2 | 2 | 0 | word (RWi) ← (ear) | — | — | — | — | — | * | * | — | — | — |
| MOVW RWi, eam | 2+ | 3+ (a) | (c) | word (RWi) ← (eam) | — | — | — | — | — | * | * | — | — | — |
| MOVW ear, RWi | 2 | 3 | 0 | word (ear) ← (RWi) | — | — | — | — | — | * | * | — | — | — |
| MOVW eam, RWi | 2+ | 3+ (a) | (c) | word (eam) ← (RWi) | — | — | — | — | — | * | * | — | — | — |
| MOVW RWi, #imm16 | 3 | 2 | 0 | word (RWi) ← imm16 | — | — | — | — | — | * | * | — | — | — |
| MOVW io, #imm16 | 4 | 3 | (c) | word (io) ← imm16 | — | — | — | — | — | — | — | — | — | — |
| MOVW ear, #imm16 | 4 | 2 | 0 | word (ear) ← imm16 | — | — | — | — | — | * | * | — | — | — |
| MOVW eam, #imm16 | 4+ | 2+ (a) | (c) | word (eam) ← imm16 | — | — | — | — | — | — | — | — | — | — |
| MOVW @AL, AH | 2 | 2 | (c) | word ((A)) ← (AH) | — | — | — | — | — | * | * | — | — | — |
| XCHW A, ear | 2 | 3 | 0 | word (A) ↔ (ear) | — | — | — | — | — | — | — | — | — | — |
| XCHW A, eam | 2+ | 3+ (a) | 2× (c) | word (A) ↔ (eam) | — | — | — | — | — | — | — | — | — | — |
| XCHW RWi, ear | 2 | 4 | 0 | word (RWi) ↔ (ear) | — | — | — | — | — | — | — | — | — | — |
| XCHW RWi, eam | 2+ | 5+ (a) | 2× (c) | word (RWi) ↔ (eam) | — | — | — | — | — | — | — | — | — | — |

Note: For an explanation of “(a)” and “(c)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 8 Transfer Instructions (Long Word) [11 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|---------------------|----|--------|-----|---------------------------|----|----|---|---|---|---|---|---|---|-----|
| MOVL A, ear | 2 | 1 | 0 | long (A) ← (ear) | – | – | – | – | – | * | * | – | – | – |
| MOVL A, eam | 2+ | 3+ (a) | (d) | long (A) ← (eam) | – | – | – | – | – | * | * | – | – | – |
| MOVL A, # imm32 | 5 | 3 | 0 | long (A) ← imm32 | – | – | – | – | – | * | * | – | – | – |
| MOVL A, @SP + disp8 | 3 | 4 | (d) | long (A) ← ((SP) + disp8) | – | – | – | – | – | * | * | – | – | – |
| MOVPL A, addr24 | 5 | 4 | (d) | long (A) ← (addr24) | – | – | – | – | – | * | * | – | – | – |
| MOVPL A, @A | 2 | 3 | (d) | long (A) ← ((A)) | – | – | – | – | – | * | * | – | – | – |
| MOVPL @A, RLi | 2 | 5 | (d) | long ((A)) ← (RLi) | – | – | – | – | – | * | * | – | – | – |
| MOVL @SP + disp8, A | 3 | 4 | (d) | long ((SP) + disp8) ← (A) | – | – | – | – | – | * | * | – | – | – |
| MOVPL addr24, A | 5 | 4 | (d) | long (addr24) ← (A) | – | – | – | – | – | * | * | – | – | – |
| MOVL ear, A | 2 | 2 | 0 | long (ear) ← (A) | – | – | – | – | – | * | * | – | – | – |
| MOVL eam, A | 2+ | 3+ (a) | (d) | long (eam) ← (A) | – | – | – | – | – | * | * | – | – | – |

For an explanation of “(a)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------------|----|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| ADD A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) +imm8 | Z | – | – | – | – | * | * | * | * | – |
| ADD A, dir | 2 | 3 | (b) | byte (A) ← (A) +(dir) | Z | – | – | – | – | * | * | * | * | – |
| ADD A, ear | 2 | 2 | 0 | byte (A) ← (A) +(ear) | Z | – | – | – | – | * | * | * | * | – |
| ADD A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) +(eam) | Z | – | – | – | – | * | * | * | * | – |
| ADD ear, A | 2 | 2 | 0 | byte (ear) ← (ear) + (A) | – | – | – | – | – | * | * | * | * | * |
| ADD eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) + (A) | Z | – | – | – | – | * | * | * | * | * |
| ADDC A | 1 | 2 | 0 | byte (A) ← (AH) + (AL) + (C) | Z | – | – | – | – | * | * | * | * | – |
| ADDC A, ear | 2 | 2 | 0 | byte (A) ← (A) + (ear) + (C) | Z | – | – | – | – | * | * | * | * | – |
| ADDC A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) + (eam) + (C) | Z | – | – | – | – | * | * | * | * | – |
| ADDC A | 1 | 3 | 0 | byte (A) ← (AH) + (AL) + (C) (Decimal) | Z | – | – | – | – | * | * | * | * | – |
| SUB A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) –imm8 | Z | – | – | – | – | * | * | * | * | – |
| SUB A, dir | 2 | 3 | (b) | byte (A) ← (A) – (dir) | Z | – | – | – | – | * | * | * | * | – |
| SUB A, ear | 2 | 2 | 0 | byte (A) ← (A) – (ear) | Z | – | – | – | – | * | * | * | * | – |
| SUB A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) – (eam) | Z | – | – | – | – | * | * | * | * | – |
| SUB ear, A | 2 | 2 | 0 | byte (ear) ← (ear) – (A) | – | – | – | – | – | * | * | * | * | * |
| SUB eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) – (A) | – | – | – | – | – | * | * | * | * | * |
| SUBC A | 1 | 2 | 0 | byte (A) ← (AH) – (AL) – (C) | Z | – | – | – | – | * | * | * | * | – |
| SUBC A, ear | 2 | 2 | 0 | byte (A) ← (A) – (ear) – (C) | Z | – | – | – | – | * | * | * | * | – |
| SUBC A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) – (eam) – (C) | Z | – | – | – | – | * | * | * | * | – |
| SUBC A | 1 | 3 | 0 | byte (A) ← (AH) – (AL) – (C) (Decimal) | Z | – | – | – | – | * | * | * | * | – |
| ADDW A | 1 | 2 | 0 | word (A) ← (AH) + (AL) | – | – | – | – | – | * | * | * | * | – |
| ADDW A, ear | 2 | 2 | 0 | word (A) ← (A) +(ear) | – | – | – | – | – | * | * | * | * | – |
| ADDW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) +(eam) | – | – | – | – | – | * | * | * | * | – |
| ADDW A, #imm16 | 3 | 2 | 0 | word (A) ← (A) +imm16 | – | – | – | – | – | * | * | * | * | – |
| ADDW ear, A | 2 | 2 | 0 | word (ear) ← (ear) + (A) | – | – | – | – | – | * | * | * | * | * |
| ADDW eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) + (A) | – | – | – | – | – | * | * | * | * | * |
| ADDCW A, ear | 2 | 2 | 0 | word (A) ← (A) + (ear) + (C) | – | – | – | – | – | * | * | * | * | – |
| ADDCW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) + (eam) + (C) | – | – | – | – | – | * | * | * | * | – |
| SUBW A | 1 | 2 | 0 | word (A) ← (AH) – (AL) | – | – | – | – | – | * | * | * | * | – |
| SUBW A, ear | 2 | 2 | 0 | word (A) ← (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| SUBW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| SUBW A, #imm16 | 3 | 2 | 0 | word (A) ← (A) –imm16 | – | – | – | – | – | * | * | * | * | – |
| SUBW ear, A | 2 | 2 | 0 | word (ear) ← (ear) – (A) | – | – | – | – | – | * | * | * | * | * |
| SUBW eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) – (A) | – | – | – | – | – | * | * | * | * | * |
| SUBCW A, ear | 2 | 2 | 0 | word (A) ← (A) – (ear) – (C) | – | – | – | – | – | * | * | * | * | – |
| SUBCW A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) – (eam) – (C) | – | – | – | – | – | * | * | * | * | – |
| ADDL A, ear | 2 | 5 | 0 | long (A) ← (A) + (ear) | – | – | – | – | – | * | * | * | * | – |
| ADDL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) + (eam) | – | – | – | – | – | * | * | * | * | – |
| ADDL A, #imm32 | 5 | 4 | 0 | long (A) ← (A) +imm32 | – | – | – | – | – | * | * | * | * | – |
| SUBL A, ear | 2 | 5 | 0 | long (A) ← (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| SUBL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| SUBL A, #imm32 | 5 | 4 | 0 | long (A) ← (A) –imm32 | – | – | – | – | – | * | * | * | * | – |

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

| Mnemonic | | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|-----|----|--------|--------|-----------------------|----|----|---|---|---|---|---|---|---|-----|
| INC | ear | 2 | 2 | 0 | byte (ear) ← (ear) +1 | – | – | – | – | – | * | * | * | – | * |
| INC | eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) +1 | – | – | – | – | – | * | * | * | – | * |
| DEC | ear | 2 | 2 | 0 | byte (ear) ← (ear) –1 | – | – | – | – | – | * | * | * | – | * |
| DEC | eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) –1 | – | – | – | – | – | * | * | * | – | * |
| INCW | ear | 2 | 2 | 0 | word (ear) ← (ear) +1 | – | – | – | – | – | * | * | * | – | * |
| INCW | eam | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) +1 | – | – | – | – | – | * | * | * | – | * |
| DECW | ear | 2 | 2 | 0 | word (ear) ← (ear) –1 | – | – | – | – | – | * | * | * | – | * |
| DECW | eam | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) –1 | – | – | – | – | – | * | * | * | – | * |
| INCL | ear | 2 | 4 | 0 | long (ear) ← (ear) +1 | – | – | – | – | – | * | * | * | – | * |
| INCL | eam | 2+ | 5+ (a) | 2× (d) | long (eam) ← (eam) +1 | – | – | – | – | – | * | * | * | – | * |
| DECL | ear | 2 | 4 | 0 | long (ear) ← (ear) –1 | – | – | – | – | – | * | * | * | – | * |
| DECL | eam | 2+ | 5+ (a) | 2× (d) | long (eam) ← (eam) –1 | – | – | – | – | – | * | * | * | – | * |

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

| Mnemonic | | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|-----------|----|--------|-----|------------------|----|----|---|---|---|---|---|---|---|-----|
| CMP | A | 1 | 2 | 0 | byte (AH) – (AL) | – | – | – | – | – | * | * | * | * | – |
| CMP | A, ear | 2 | 2 | 0 | byte (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| CMP | A, eam | 2+ | 2+ (a) | (b) | byte (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| CMP | A, #imm8 | 2 | 2 | 0 | byte (A) – imm8 | – | – | – | – | – | * | * | * | * | – |
| CMPW | A | 1 | 2 | 0 | word (AH) – (AL) | – | – | – | – | – | * | * | * | * | – |
| CMPW | A, ear | 2 | 2 | 0 | word (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| CMPW | A, eam | 2+ | 2+ (a) | (c) | word (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| CMPW | A, #imm16 | 3 | 2 | 0 | word (A) – imm16 | – | – | – | – | – | * | * | * | * | – |
| CMPL | A, ear | 2 | 3 | 0 | long (A) – (ear) | – | – | – | – | – | * | * | * | * | – |
| CMPL | A, eam | 2+ | 4+ (a) | (d) | long (A) – (eam) | – | – | – | – | – | * | * | * | * | – |
| CMPL | A, #imm32 | 5 | 3 | 0 | long (A) – imm32 | – | – | – | – | – | * | * | * | * | – |

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 12 Unsigned Multiplication and Division Instructions (Word/Long Word) [11 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|--------------|----|--------|-----|--|----|----|---|---|---|---|---|---|---|-----|
| DIVU A | 1 | *1 | 0 | word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH) | — | — | — | — | — | — | — | * | * | — |
| DIVU A, ear | 2 | *2 | 0 | word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear) | — | — | — | — | — | — | — | * | * | — |
| DIVU A, eam | 2+ | *3 | *6 | word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam) | — | — | — | — | — | — | — | * | * | — |
| DIVUW A, ear | 2 | *4 | 0 | long (A)/word (ear) Quotient → word (A) Remainder → word (ear) | — | — | — | — | — | — | — | * | * | — |
| DIVUW A, eam | 2+ | *5 | *7 | long (A)/word (eam) Quotient → word (A) Remainder → word (eam) | — | — | — | — | — | — | — | * | * | — |
| MULU A | 1 | *8 | 0 | byte (AH) × byte (AL) → word (A) | — | — | — | — | — | — | — | — | — | — |
| MULU A, ear | 2 | *9 | 0 | byte (A) × byte (ear) → word (A) | — | — | — | — | — | — | — | — | — | — |
| MULU A, eam | 2+ | *10 | (b) | byte (A) × byte (eam) → word (A) | — | — | — | — | — | — | — | — | — | — |
| MULUW A | 1 | *11 | 0 | word (AH) × word (AL) → long (A) | — | — | — | — | — | — | — | — | — | — |
| MULUW A, ear | 2 | *12 | 0 | word (A) × word (ear) → long (A) | — | — | — | — | — | — | — | — | — | — |
| MULUW A, eam | 2+ | *13 | (c) | word (A) × word (eam) → long (A) | — | — | — | — | — | — | — | — | — | — |

For an explanation of “(b)” and “(c), refer to Table 5, “Correction Values for Number of Cycle Used to Calculate Number of Actual Cycles.”

- *1: 3 when dividing into zero, 6 when an overflow occurs, and 14 normally.
- *2: 3 when dividing into zero, 5 when an overflow occurs, and 13 normally.
- *3: 5 + (a) when dividing into zero, 7 + (a) when an overflow occurs, and 17 + (a) normally.
- *4: 3 when dividing into zero, 5 when an overflow occurs, and 21 normally.
- *5: 4 + (a) when dividing into zero, 7 + (a) when an overflow occurs, and 25 + (a) normally.
- *6: (b) when dividing into zero or when an overflow occurs, and 2 × (b) normally.
- *7: (c) when dividing into zero or when an overflow occurs, and 2 × (c) normally.
- *8: 3 when byte (AH) is zero, and 7 when byte (AH) is not 0.
- *9: 3 when byte (ear) is zero, and 7 when byte (ear) is not 0.
- *10: 4 + (a) when byte (eam) is zero, and 8 + (a) when byte (eam) is not 0.
- *11: 3 when word (AH) is zero, and 11 when word (AH) is not 0.
- *12: 3 when word (ear) is zero, and 11 when word (ear) is not 0.
- *13: 4 + (a) when word (eam) is zero, and 12 + (a) when word (eam) is not 0.

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Table 13 Signed Multiplication and Division Instructions (Word/Long Word) [11 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|-------------|----|--------|-----|--|----|----|---|---|---|---|---|---|---|-----|
| DIV A | 2 | *1 | 0 | word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH) | Z | – | – | – | – | – | – | * | * | – |
| DIV A, ear | 2 | *2 | 0 | word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear) | Z | – | – | – | – | – | – | * | * | – |
| DIV A, eam | 2+ | *3 | *6 | word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam) | Z | – | – | – | – | – | – | * | * | – |
| DIVWA, ear | 2 | *4 | 0 | long (A)/word (ear) Quotient → word (A) Remainder → word (ear) | – | – | – | – | – | – | – | * | * | – |
| DIVWA, eam | 2+ | *5 | *7 | long (A)/word (eam) Quotient → word (A) Remainder → word (eam) | – | – | – | – | – | – | – | * | * | – |
| MUL A | 2 | *8 | 0 | byte (AH) × byte (AL) → word (A) | – | – | – | – | – | – | – | – | – | – |
| MUL A, ear | 2 | *9 | 0 | byte (A) × byte (ear) → word (A) | – | – | – | – | – | – | – | – | – | – |
| MUL A, eam | 2+ | *10 | (b) | byte (A) × byte (eam) → word (A) | – | – | – | – | – | – | – | – | – | – |
| MULW A | 2 | *11 | 0 | word (AH) × word (AL) → long (A) | – | – | – | – | – | – | – | – | – | – |
| MULW A, ear | 2 | *12 | 0 | word (A) × word (ear) → long (A) | – | – | – | – | – | – | – | – | – | – |
| MULW A, eam | 2+ | *13 | (b) | word (A) × word (eam) → long (A) | – | – | – | – | – | – | – | – | – | – |

For an explanation of “(b)” and “(c)”, refer to Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 3 when dividing into zero, 8 or 18 when an overflow occurs, and 18 normally.

*2: 3 when dividing into zero, 10 or 21 when an overflow occurs, and 22 normally.

*3: 4 + (a) when dividing into zero, 11 + (a) or 22 + (a) when an overflow occurs, and 23 + (a) normally.

*4: When the dividend is positive: 4 when dividing into zero, 10 or 29 when an overflow occurs, and 30 normally.
When the dividend is negative: 4 when dividing into zero, 11 or 30 when an overflow occurs, and 31 normally.

*5: When the dividend is positive: 4 + (a) when dividing into zero, 11 + (a) or 30 + (a) when an overflow occurs, and 31 + (a) normally.

When the dividend is negative: 4 + (a) when dividing into zero, 12 + (a) or 31 + (a) when an overflow occurs, and 32 + (a) normally.

*6: (b) when dividing into zero or when an overflow occurs, and 2 × (b) normally.

*7: (c) when dividing into zero or when an overflow occurs, and 2 × (c) normally.

*8: 3 when byte (AH) is zero, 12 when the result is positive, and 13 when the result is negative.

*9: 3 when byte (ear) is zero, 12 when the result is positive, and 13 when the result is negative.

*10: 4 + (a) when byte (eam) is zero, 13 + (a) when the result is positive, and 14 + (a) when the result is negative.

*11: 3 when word (AH) is zero, 12 when the result is positive, and 13 when the result is negative.

*12: 3 when word (ear) is zero, 16 when the result is positive, and 19 when the result is negative.

*13: 4 + (a) when word (eam) is zero, 17 + (a) when the result is positive, and 20 + (a) when the result is negative.

Note: Which of the two values given for the number of execution cycles applies when an overflow error occurs in a DIV or DIVW instruction depends on whether the overflow was detected before or after the operation.

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Table 14 Logical 1 Instructions (Byte, Word) [39 Instructions]

| Mnemonic | | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|-----------|----|--------|--------|----------------------------|----|----|---|---|---|---|---|---|---|-----|
| AND | A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) and imm8 | — | — | — | — | — | * | * | R | — | — |
| AND | A, ear | 2 | 2 | 0 | byte (A) ← (A) and (ear) | — | — | — | — | — | * | * | R | — | — |
| AND | A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) and (eam) | — | — | — | — | — | * | * | R | — | — |
| AND | ear, A | 2 | 3 | 0 | byte (ear) ← (ear) and (A) | — | — | — | — | — | * | * | R | — | * |
| AND | eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) and (A) | — | — | — | — | — | * | * | R | — | * |
| OR | A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) or imm8 | — | — | — | — | — | * | * | R | — | — |
| OR | A, ear | 2 | 2 | 0 | byte (A) ← (A) or (ear) | — | — | — | — | — | * | * | R | — | — |
| OR | A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) or (eam) | — | — | — | — | — | * | * | R | — | — |
| OR | ear, A | 2 | 3 | 0 | byte (ear) ← (ear) or (A) | — | — | — | — | — | * | * | R | — | * |
| OR | eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) or (A) | — | — | — | — | — | * | * | R | — | * |
| XOR | A, #imm8 | 2 | 2 | 0 | byte (A) ← (A) xor imm8 | — | — | — | — | — | * | * | R | — | — |
| XOR | A, ear | 2 | 2 | 0 | byte (A) ← (A) xor (ear) | — | — | — | — | — | * | * | R | — | — |
| XOR | A, eam | 2+ | 3+ (a) | (b) | byte (A) ← (A) xor (eam) | — | — | — | — | — | * | * | R | — | — |
| XOR | ear, A | 2 | 3 | 0 | byte (ear) ← (ear) xor (A) | — | — | — | — | — | * | * | R | — | * |
| XOR | eam, A | 2+ | 3+ (a) | 2× (b) | byte (eam) ← (eam) xor (A) | — | — | — | — | — | * | * | R | — | * |
| NOT | A | 1 | 2 | 0 | byte (A) ← not (A) | — | — | — | — | — | * | * | R | — | — |
| NOT | ear | 2 | 2 | 0 | byte (ear) ← not (ear) | — | — | — | — | — | * | * | R | — | * |
| NOT | eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← not (eam) | — | — | — | — | — | * | * | R | — | * |
| ANDW | A | 1 | 2 | 0 | word (A) ← (AH) and (A) | — | — | — | — | — | * | * | R | — | — |
| ANDW | A, #imm16 | 3 | 2 | 0 | word (A) ← (A) and imm16 | — | — | — | — | — | * | * | R | — | — |
| ANDW | A, ear | 2 | 2 | 0 | word (A) ← (A) and (ear) | — | — | — | — | — | * | * | R | — | — |
| ANDW | A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) and (eam) | — | — | — | — | — | * | * | R | — | — |
| ANDW | ear, A | 2 | 3 | 0 | word (ear) ← (ear) and (A) | — | — | — | — | — | * | * | R | — | * |
| ANDW | eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) and (A) | — | — | — | — | — | * | * | R | — | * |
| ORW | A | 1 | 2 | 0 | word (A) ← (AH) or (A) | — | — | — | — | — | * | * | R | — | — |
| ORW | A, #imm16 | 3 | 2 | 0 | word (A) ← (A) or imm16 | — | — | — | — | — | * | * | R | — | — |
| ORW | A, ear | 2 | 2 | 0 | word (A) ← (A) or (ear) | — | — | — | — | — | * | * | R | — | — |
| ORW | A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) or (eam) | — | — | — | — | — | * | * | R | — | — |
| ORW | ear, A | 2 | 3 | 0 | word (ear) ← (ear) or (A) | — | — | — | — | — | * | * | R | — | * |
| ORW | eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) or (A) | — | — | — | — | — | * | * | R | — | * |
| XORW | A | 1 | 2 | 0 | word (A) ← (AH) xor (A) | — | — | — | — | — | * | * | R | — | — |
| XORW | A, #imm16 | 3 | 2 | 0 | word (A) ← (A) xor imm16 | — | — | — | — | — | * | * | R | — | — |
| XORW | A, ear | 2 | 2 | 0 | word (A) ← (A) xor (ear) | — | — | — | — | — | * | * | R | — | — |
| XORW | A, eam | 2+ | 3+ (a) | (c) | word (A) ← (A) xor (eam) | — | — | — | — | — | * | * | R | — | — |
| XORW | ear, A | 2 | 3 | 0 | word (ear) ← (ear) xor (A) | — | — | — | — | — | * | * | R | — | * |
| XORW | eam, A | 2+ | 3+ (a) | 2× (c) | word (eam) ← (eam) xor (A) | — | — | — | — | — | * | * | R | — | * |
| NOTW | A | 1 | 2 | 0 | word (A) ← not (A) | — | — | — | — | — | * | * | R | — | — |
| NOTW | ear | 2 | 2 | 0 | word (ear) ← not (ear) | — | — | — | — | — | * | * | R | — | * |
| NOTW | eam | 2+ | 3+ (a) | 2× (c) | word (eam) ← not (eam) | — | — | — | — | — | * | * | R | — | * |

For an explanation of “(a)”, “(b)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

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Table 15 Logical 2 Instructions (Long Word) [6 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|-------------|----|--------|-----|--------------------------|----|----|---|---|---|---|---|---|---|-----|
| ANDL A, ear | 2 | 5 | 0 | long (A) ← (A) and (ear) | – | – | – | – | – | * | * | R | – | – |
| ANDL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) and (eam) | – | – | – | – | – | * | * | R | – | – |
| ORL A, ear | 2 | 5 | 0 | long (A) ← (A) or (ear) | – | – | – | – | – | * | * | R | – | – |
| ORL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) or (eam) | – | – | – | – | – | * | * | R | – | – |
| XORL A, ear | 2 | 5 | 0 | long (A) ← (A) xor (ear) | – | – | – | – | – | * | * | R | – | – |
| XORL A, eam | 2+ | 6+ (a) | (d) | long (A) ← (A) xor (eam) | – | – | – | – | – | * | * | R | – | – |

For an explanation of “(a)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 16 Sign Inversion Instructions (Byte/Word) [6 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|----|--------|--------|------------------------|----|----|---|---|---|---|---|---|---|-----|
| NEG A | 1 | 2 | 0 | byte (A) ← 0 – (A) | X | – | – | – | – | * | * | * | * | – |
| NEG ear | 2 | 2 | 0 | byte (ear) ← 0 – (ear) | – | – | – | – | – | * | * | * | * | * |
| NEG eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← 0 – (eam) | – | – | – | – | – | * | * | * | * | * |
| NEGW A | 1 | 2 | 0 | word (A) ← 0 – (A) | – | – | – | – | – | * | * | * | * | – |
| NEGW ear | 2 | 2 | 0 | word (ear) ← 0 – (ear) | – | – | – | – | – | * | * | * | * | * |
| NEGW eam | 2+ | 3+ (a) | 2× (c) | word (eam) ← 0 – (eam) | – | – | – | – | – | * | * | * | * | * |

For an explanation of “(a)”, “(b)” and “(c)” and refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 17 Absolute Value Instructions (Byte/Word/Long Word) [3 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|---|--------|---|-------------------------------|----|----|---|---|---|---|---|---|---|-----|
| ABS A | 2 | 2 | 0 | byte (A) ← absolute value (A) | Z | – | – | – | – | * | * | * | – | – |
| ABSW A | 2 | 2 | 0 | word (A) ← absolute value (A) | – | – | – | – | – | * | * | * | – | – |
| ABSL A | 2 | 4 | 0 | long (A) ← absolute value (A) | – | – | – | – | – | * | * | * | – | – |

Table 18 Normalize Instructions (Long Word) [1 Instruction]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|------------|---|--------|---|---|----|----|---|---|---|---|---|---|---|-----|
| NRML A, R0 | 2 | * | 0 | long (A) ← Shifts to the position at which “1” was set first byte (R0) ← current shift count | – | – | – | – | * | – | – | – | – | – |

* : 5 when the contents of the accumulator are all zeroes, 5 + (R0) in all other cases.

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Table 19 Shift Instructions (Byte/Word/Long Word) [27 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|---------------|----|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| RORC A | 2 | 2 | 0 | byte (A) ← Right rotation with carry | – | – | – | – | – | * | * | – | * | – |
| ROLC A | 2 | 2 | 0 | byte (A) ← Left rotation with carry | – | – | – | – | – | * | * | – | * | – |
| RORC ear | 2 | 2 | 0 | byte (ear) ← Right rotation with carry | – | – | – | – | – | * | * | – | * | * |
| RORC eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← Right rotation with carry | – | – | – | – | – | * | * | – | * | * |
| ROLC ear | 2 | 2 | 0 | byte (ear) ← Left rotation with carry | – | – | – | – | – | * | * | – | * | * |
| ROLC eam | 2+ | 3+ (a) | 2× (b) | byte (eam) ← Left rotation with carry | – | – | – | – | – | * | * | – | * | * |
| ASR A, R0 | 2 | *1 | 0 | byte (A) ← Arithmetic right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSR A, R0 | 2 | *1 | 0 | byte (A) ← Logical right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSL A, R0 | 2 | *1 | 0 | byte (A) ← Logical left barrel shift (A, R0) | – | – | – | – | – | * | * | – | * | – |
| ASR A, #imm8 | 3 | *3 | 0 | byte (A) ← Arithmetic right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSR A, #imm8 | 3 | *3 | 0 | byte (A) ← Logical right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSL A, #imm8 | 3 | *3 | 0 | byte (A) ← Logical left barrel shift (A, imm8) | – | – | – | – | – | * | * | – | * | – |
| ASRW A | 1 | 2 | 0 | word (A) ← Arithmetic right shift (A, 1 bit) | – | – | – | – | * | * | * | – | * | – |
| LSRW A/SHRW A | 1 | 2 | 0 | word (A) ← Logical right shift (A, 1 bit) | – | – | – | – | * | R | * | – | * | – |
| LSLW A/SHLW A | 1 | 2 | 0 | word (A) ← Logical left shift (A, 1 bit) | – | – | – | – | – | * | * | – | * | – |
| ASRW A, R0 | 2 | *1 | 0 | word (A) ← Arithmetic right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSRW A, R0 | 2 | *1 | 0 | word (A) ← Logical right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSLW A, R0 | 2 | *1 | 0 | word (A) ← Logical left barrel shift (A, R0) | – | – | – | – | – | * | * | – | * | – |
| ASRW A, #imm8 | 3 | *3 | 0 | word (A) ← Arithmetic right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSRW A, #imm8 | 3 | *3 | 0 | word (A) ← Logical right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSLW A, #imm8 | 3 | *3 | 0 | word (A) ← Logical left barrel shift (A, imm8) | – | – | – | – | – | * | * | – | * | – |
| ASRL A, R0 | 2 | *2 | 0 | long (A) ← Arithmetic right shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSRL A, R0 | 2 | *2 | 0 | long (A) ← Logical right barrel shift (A, R0) | – | – | – | – | * | * | * | – | * | – |
| LSLL A, R0 | 2 | *2 | 0 | long (A) ← Logical left barrel shift (A, R0) | – | – | – | – | – | * | * | – | * | – |
| ASRL A, #imm8 | 3 | *4 | 0 | long (A) ← Arithmetic right shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSRL A, #imm8 | 3 | *4 | 0 | long (A) ← Logical right barrel shift (A, imm8) | – | – | – | – | * | * | * | – | * | – |
| LSLL A, #imm8 | 3 | *4 | 0 | long (A) ← Logical left barrel shift (A, imm8) | – | – | – | – | – | * | * | – | * | – |

For an explanation of “(a)” and “(b)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 3 when R0 is 0, 3 + (R0) in all other cases.

*2: 3 when R0 is 0, 4 + (R0) in all other cases.

*3: 3 when imm8 is 0, 3 + (imm8) in all other cases.

*4: 3 when imm8 is 0, 4 + (imm8) in all other cases.

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Table 20 Branch 1 Instructions [31 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|-----------------|----|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| BZ/BEQ rel | 2 | *1 | 0 | Branch when (Z) = 1 | - | - | - | - | - | - | - | - | - | - |
| BNZ/BNE rel | 2 | *1 | 0 | Branch when (Z) = 0 | - | - | - | - | - | - | - | - | - | - |
| BC/BLO rel | 2 | *1 | 0 | Branch when (C) = 1 | - | - | - | - | - | - | - | - | - | - |
| BNC/BHS rel | 2 | *1 | 0 | Branch when (C) = 0 | - | - | - | - | - | - | - | - | - | - |
| BN rel | 2 | *1 | 0 | Branch when (N) = 1 | - | - | - | - | - | - | - | - | - | - |
| BP rel | 2 | *1 | 0 | Branch when (N) = 0 | - | - | - | - | - | - | - | - | - | - |
| BV rel | 2 | *1 | 0 | Branch when (V) = 1 | - | - | - | - | - | - | - | - | - | - |
| BNV rel | 2 | *1 | 0 | Branch when (V) = 0 | - | - | - | - | - | - | - | - | - | - |
| BT rel | 2 | *1 | 0 | Branch when (T) = 1 | - | - | - | - | - | - | - | - | - | - |
| BNT rel | 2 | *1 | 0 | Branch when (T) = 0 | - | - | - | - | - | - | - | - | - | - |
| BLT rel | 2 | *1 | 0 | Branch when (V) xor (N) = 1 | - | - | - | - | - | - | - | - | - | - |
| BGE rel | 2 | *1 | 0 | Branch when (V) xor (N) = 0 | - | - | - | - | - | - | - | - | - | - |
| BLE rel | 2 | *1 | 0 | ((V) xor (N)) or (Z) = 1 | - | - | - | - | - | - | - | - | - | - |
| BGT rel | 2 | *1 | 0 | ((V) xor (N)) or (Z) = 0 | - | - | - | - | - | - | - | - | - | - |
| BLS rel | 2 | *1 | 0 | Branch when (C) or (Z) = 1 | - | - | - | - | - | - | - | - | - | - |
| BHI rel | 2 | *1 | 0 | Branch when (C) or (Z) = 0 | - | - | - | - | - | - | - | - | - | - |
| BRA rel | 2 | *1 | 0 | Branch unconditionally | - | - | - | - | - | - | - | - | - | - |
| JMP @A | 1 | 2 | 0 | word (PC) ← (A) | - | - | - | - | - | - | - | - | - | - |
| JMP addr16 | 3 | 2 | 0 | word (PC) ← addr16 | - | - | - | - | - | - | - | - | - | - |
| JMP @ear | 2 | 3 | 0 | word (PC) ← (ear) | - | - | - | - | - | - | - | - | - | - |
| JMP @eam | 2+ | 4+ (a) | (c) | word (PC) ← (eam) | - | - | - | - | - | - | - | - | - | - |
| JMPP @ear *3 | 2 | 3 | 0 | word (PC) ← (ear), (PCB) ← (ear +2) | - | - | - | - | - | - | - | - | - | - |
| JMPP @eam *3 | 2+ | 4+ (a) | (d) | word (PC) ← (eam), (PCB) ← (eam +2) | - | - | - | - | - | - | - | - | - | - |
| JMPP addr24 | 4 | 3 | 0 | word (PC) ← ad24 0 to 15 (PCB) ← ad24 16 to 23 | - | - | - | - | - | - | - | - | - | - |
| CALL @ear *4 | 2 | 4 | (c) | word (PC) ← (ear) | - | - | - | - | - | - | - | - | - | - |
| CALL @eam *4 | 2+ | 5+ (a) | 2× (c) | word (PC) ← (eam) | - | - | - | - | - | - | - | - | - | - |
| CALL addr16 *5 | 3 | 5 | (c) | word (PC) ← addr16 | - | - | - | - | - | - | - | - | - | - |
| CALLV #vct4 *5 | 1 | 5 | 2× (c) | Vector call instruction | - | - | - | - | - | - | - | - | - | - |
| CALLP @ear *6 | 2 | 7 | 2× (c) | word (PC) ← (ear) 0 to 15, (PCB) ← (ear) 16 to 23 | - | - | - | - | - | - | - | - | - | - |
| CALLP @eam *6 | 2+ | 8+ (a) | *2 | word (PC) ← (eam) 0 to 15, (PCB) ← (eam) 16 to 23 | - | - | - | - | - | - | - | - | - | - |
| CALLP addr24 *7 | 4 | 7 | 2× (c) | word (PC) ← addr 0 to 15, (PCB) ← addr 16 to 23 | - | - | - | - | - | - | - | - | - | - |

For an explanation of “(a)”, “(c)” and “(d)”, refer to Table 4, “Number of Execution Cycles for Each Form of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 3 when branching, 2 when not branching.

*2: $3 \times (c) + (b)$

*3: Read (word) branch address.

*4: W: Save (word) to stack; R: Read (word) branch address.

*5: Save (word) to stack.

*6: W: Save (long word) to W stack; R: Read (long word) branch address.

*7: Save (long word) to stack.

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Table 21 Branch 2 Instructions [20 Instructions]

| Mnemonic | # | cycle | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|------------------------|----|-------|----------------|--|----|----|---|---|---|---|---|---|---|-----|
| CBNE A, #imm8, rel | 3 | *1 | 0 | Branch when byte (A) \neq imm8 | — | — | — | — | — | * | * | * | * | — |
| CWBNE A, #imm16, rel | 4 | *1 | 0 | Branch when byte (A) \neq imm16 | — | — | — | — | — | * | * | * | * | — |
| CBNE ear, #imm8, rel | 4 | *3 | 0 | Branch when byte (ear) \neq imm8 | — | — | — | — | — | * | * | * | * | — |
| CBNE eam, #imm8, rel | 4+ | *1 | (b) | Branch when byte (eam) \neq imm8 | — | — | — | — | — | * | * | * | * | — |
| CWBNE ear, #imm16, rel | 5 | *3 | 0 | Branch when word (ear) \neq imm16 | — | — | — | — | — | * | * | * | * | — |
| CWBNE eam, #imm16, rel | 5+ | *2 | (c) | Branch when word (eam) \neq imm16 | — | — | — | — | — | * | * | * | * | — |
| DBNZ ear, rel | 3 | *4 | 0 | Branch when byte (ear) = (ear) - 1, and (ear) \neq 0 | — | — | — | — | — | * | * | * | — | — |
| DBNZ eam, rel | 3+ | *2 | 2 \times (b) | Branch when byte (ear) = (eam) - 1, and (eam) \neq 0 | — | — | — | — | — | * | * | * | — | * |
| DWBNZ ear, rel | 3 | *4 | 0 | Branch when word (ear) = (ear) - 1, and (ear) \neq 0 | — | — | — | — | — | * | * | * | — | — |
| DWBNZ eam, rel | 3+ | | 2 \times (c) | Branch when word (eam) = (eam) - 1, and (eam) \neq 0 | — | — | — | — | — | * | * | * | — | * |
| | | 14 | | | | | | | | | | | | |
| | | 12 | | | | | | | | | | | | |
| INT #vct8 | 2 | 13 | 8 \times (c) | Software interrupt | — | — | R | S | — | — | — | — | — | — |
| INT addr16 | 3 | 14 | 6 \times (c) | Software interrupt | — | — | R | S | — | — | — | — | — | — |
| INTP addr24 | 4 | 9 | 6 \times (c) | Software interrupt | — | — | R | S | — | — | — | — | — | — |
| INT9 | 1 | 11 | 8 \times (c) | Software interrupt | — | — | R | S | — | — | — | — | — | — |
| RETI | 1 | | 6 \times (c) | Return from interrupt | — | — | * | * | * | * | * | * | * | — |
| RETIQ *6 | 2 | 6 | *5 | Return from interrupt | — | — | * | * | * | * | * | * | * | — |
| LINK #imm8 | 2 | | (c) | At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area | — | — | — | — | — | — | — | — | — | — |
| | | 5 | | | | | | | | | | | | |
| UNLINK | 1 | | (c) | At constant entry, retrieve old frame pointer from stack. | — | — | — | — | — | — | — | — | — | — |
| | | 4 | | | | | | | | | | | | |
| | | 5 | | | | | | | | | | | | |
| RET *7 | 1 | | (c) | Return from subroutine | — | — | — | — | — | — | — | — | — | — |
| RETP *8 | 1 | | (d) | Return from subroutine | — | — | — | — | — | — | — | — | — | — |

For an explanation of “(b)”, “(c)” and “(d)”, refer to Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 4 when branching, 3 when not branching

*2: 5 when branching, 4 when not branching

*3: 5 + (a) when branching, 4 + (a) when not branching

*4: 6 + (a) when branching, 5 + (a) when not branching

*5: 3 \times (b) + 2 \times (c) when an interrupt request is generated, 6 \times (c) when returning from the interrupt.

*6: High-speed interrupt return instruction. When an interrupt request is detected during this instruction, the instruction branches to the interrupt vector without performing stack operations when the interrupt is generated.

*7: Return from stack (word)

*8: Return from stack (long word)

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Table 22 Other Control Instructions (Byte/Word/Long Word) [36 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|-------------------|----|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| PUSHW A | 1 | 3 | (c) | word (SP) ← (SP) - 2, ((SP)) ← (A) | - | - | - | - | - | - | - | - | - | - |
| PUSHW AH | 1 | 3 | (c) | word (SP) ← (SP) - 2, ((SP)) ← (AH) | - | - | - | - | - | - | - | - | - | - |
| PUSHW PS | 1 | 3 | (c) | word (SP) ← (SP) - 2, ((SP)) ← (PS) | - | - | - | - | - | - | - | - | - | - |
| PUSHW rlst | 2 | *3 | *4 | (SP) ← (SP) - 2n, ((SP)) ← (rlst) | - | - | - | - | - | - | - | - | - | - |
| POPW A | 1 | 3 | (c) | word (A) ← ((SP)), (SP) ← (SP) + 2 | - | * | - | - | - | - | - | - | - | - |
| POPW AH | 1 | 3 | (c) | word (AH) ← ((SP)), (SP) ← (SP) + 2 | - | - | - | - | - | - | - | - | - | - |
| POPW PS | 1 | 3 | (c) | word (PS) ← ((SP)), (SP) ← (SP) + 2 | - | - | * | * | * | * | * | * | * | - |
| POPW rlst | 2 | *2 | *4 | (rlst) ← ((SP)), (SP) ← (SP) | - | - | - | - | - | - | - | - | - | - |
| JCTX @A | 1 | 9 | 6× (c) | Context switch instruction | - | - | * | * | * | * | * | * | * | - |
| AND CCR, #imm8 | 2 | 3 | 0 | byte (CCR) ← (CCR) and imm8 | - | - | * | * | * | * | * | * | * | - |
| OR CCR, #imm8 | 2 | 3 | 0 | byte (CCR) ← (CCR) or imm8 | - | - | * | * | * | * | * | * | * | - |
| MOV RP, #imm8 | 2 | 2 | 0 | byte (RP) ← imm8 | - | - | - | - | - | - | - | - | - | - |
| MOV ILM, #imm8 | 2 | 2 | 0 | byte (ILM) ← imm8 | - | - | - | - | - | - | - | - | - | - |
| MOVEA RWi, ear | 2 | 3 | 0 | word (RWi) ← ear | - | - | - | - | - | - | - | - | - | - |
| MOVEA RWi, eam | 2+ | 2+ (a) | 0 | word (RWi) ← eam | - | - | - | - | - | - | - | - | - | - |
| MOVEA A, ear | 2 | 2 | 0 | word(A) ← ear | - | * | - | - | - | - | - | - | - | - |
| MOVEA A, eam | 2+ | 1+ (a) | 0 | word (A) ← eam | - | * | - | - | - | - | - | - | - | - |
| ADDSP #imm8 | 2 | 3 | 0 | word (SP) ← ext (imm8) | - | - | - | - | - | - | - | - | - | - |
| ADDSP #imm16 | 3 | 3 | 0 | word (SP) ← imm16 | - | - | - | - | - | - | - | - | - | - |
| MOV A, brgl | 2 | *1 | 0 | byte (A) ← (brgl) | Z | * | - | - | - | * | * | - | - | - |
| MOV brg2, A | 2 | 1 | 0 | byte (brg2) ← (A) | - | - | - | - | - | * | * | - | - | - |
| MOV brg2, #imm8 | 3 | 2 | 0 | byte (brg2) ← imm8 | - | - | - | - | - | * | * | - | - | - |
| NOP | 1 | 1 | 0 | No operation | - | - | - | - | - | - | - | - | - | - |
| ADB | 1 | 1 | 0 | Prefix code for AD space access | - | - | - | - | - | - | - | - | - | - |
| DTB | 1 | 1 | 0 | Prefix code for DT space access | - | - | - | - | - | - | - | - | - | - |
| PCB | 1 | 1 | 0 | Prefix code for PC space access | - | - | - | - | - | - | - | - | - | - |
| SPB | 1 | 1 | 0 | Prefix code for SP space access | - | - | - | - | - | - | - | - | - | - |
| NCC | 1 | 1 | 0 | Prefix code for no flag change | - | - | - | - | - | - | - | - | - | - |
| CMR | 1 | 1 | 0 | Prefix code for the common register bank | - | - | - | - | - | - | - | - | - | - |
| MOVW SPCU, #imm16 | 4 | 2 | 0 | word (SPCU) ← (imm16) | - | - | - | - | - | - | - | - | - | - |
| MOVW SPCL, #imm16 | 4 | 2 | 0 | word (SPCL) ← (imm16) | - | - | - | - | - | - | - | - | - | - |
| SETSPC | 2 | 2 | 0 | Stack check operation enable | - | - | - | - | - | - | - | - | - | - |
| CLRSPC | 2 | 2 | 0 | Stack check operation disable | - | - | - | - | - | - | - | - | - | - |
| BTSCN A | 2 | *5 | 0 | byte (A) ← position of "1" bit in word (A) | Z | - | - | - | - | - | * | - | - | - |
| BTSCNS A | 2 | *6 | 0 | byte (A) ← position of "1" bit in word (A) × 2 | Z | - | - | - | - | - | * | - | - | - |
| BTSCND A | 2 | *7 | 0 | byte (A) ← position of "1" bit in word (A) × 4 | Z | - | - | - | - | - | * | - | - | - |

For an explanation of "(a)" and "(c)", refer to Tables 4 and 5.

*1: PCB, ADB, SSB, USB, and SPB: 1 cycle

DTB: 2 cycles

DPR: 3 cycles

*2: 3 + 4 × (pop count)

*3: 3 + 4 × (push count)

*4: Pop count × (c), or push count × (c)

*5: 3 when AL is 0, 5 when AL is not 0.

*6: 4 when AL is 0, 6 when AL is not 0.

*7: 5 when AL is 0, 7 when AL is not 0.

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Table 23 Bit Manipulation Instructions [21 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|---------------------|---|--------|--------|--|----|----|---|---|---|---|---|---|---|-----|
| MOVB A, dir:bp | 3 | 3 | (b) | byte (A) ← (dir:bp) b | Z | * | — | — | — | * | * | — | — | — |
| MOVB A, addr16:bp | 4 | 3 | (b) | byte (A) ← (addr16:bp) b | Z | * | — | — | — | * | * | — | — | — |
| MOVB A, io:bp | 3 | 3 | (b) | byte (A) ← (io:bp) b | Z | * | — | — | — | * | * | — | — | — |
| MOVB dir:bp, A | 3 | 4 | 2× (b) | bit (dir:bp) b ← (A) | — | — | — | — | — | * | * | — | — | * |
| MOVB addr16:bp, A | 4 | 4 | 2× (b) | bit (addr16:bp) b ← (A) | — | — | — | — | — | * | * | — | — | * |
| MOVB io:bp, A | 3 | 4 | 2× (b) | bit (io:bp) b ← (A) | — | — | — | — | — | * | * | — | — | * |
| SETB dir:bp | 3 | 4 | 2× (b) | bit (dir:bp) b ← 1 | — | — | — | — | — | — | — | — | — | * |
| SETB addr16:bp | 4 | 4 | 2× (b) | bit (addr16:bp) b ← 1 | — | — | — | — | — | — | — | — | — | * |
| SETB io:bp | 3 | 4 | 2× (b) | bit (io:bp) b ← 1 | — | — | — | — | — | — | — | — | — | * |
| CLRB dir:bp | 3 | 4 | 2× (b) | bit (dir:bp) b ← 0 | — | — | — | — | — | — | — | — | — | * |
| CLRB addr16:bp | 4 | 4 | 2× (b) | bit (addr16:bp) b ← 0 | — | — | — | — | — | — | — | — | — | * |
| CLRB io:bp | 3 | 4 | 2× (b) | bit (io:bp) b ← 0 | — | — | — | — | — | — | — | — | — | * |
| BBC dir:bp, rel | 4 | *1 | (b) | Branch when (dir:bp) b = 0 | — | — | — | — | — | — | * | — | — | — |
| BBC addr16:bp, rel | 5 | *1 | (b) | Branch when (addr16:bp) b = 0 | — | — | — | — | — | — | * | — | — | — |
| BBC io:bp, rel | 4 | *1 | (b) | Branch when (io:bp) b = 0 | — | — | — | — | — | — | * | — | — | — |
| BBS dir:bp, rel | 4 | *1 | (b) | Branch when (dir:bp) b = 1 | — | — | — | — | — | — | * | — | — | — |
| BBS addr16:bp, rel | 5 | *1 | (b) | Branch when (addr16:bp) b = 1 | — | — | — | — | — | — | * | — | — | — |
| BBS io:bp, rel | 4 | *1 | (b) | Branch when (io:bp) b = 1 | — | — | — | — | — | — | * | — | — | — |
| SBBS addr16:bp, rel | 5 | *2 | 2× (b) | Branch when (addr16:bp) b = 1, bit = 1 | — | — | — | — | — | — | * | — | — | * |
| WBTS io:bp | 3 | *3 | *4 | Wait until (io:bp) b = 1 | — | — | — | — | — | — | — | — | — | — |
| WBTC io:bp | 3 | *3 | *4 | Wait until (io:bp) b = 0 | — | — | — | — | — | — | — | — | — | — |

For an explanation of “(b)”, refer to Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

*1: 5 when branching, 4 when not branching

*2: 7 when condition is satisfied, 6 when not satisfied

*3: Undefined count

*4: Until condition is satisfied

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Table 24 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|----------|---|--------|---|---|----|----|---|---|---|---|---|---|---|-----|
| SWAP | 1 | 3 | 0 | byte (A) 0 to 7 \leftrightarrow (A) 8 to 15 | - | - | - | - | - | - | - | - | - | - |
| SWAPW | 1 | 2 | 0 | word (AH) \leftrightarrow (AL) | - | * | - | - | - | - | - | - | - | - |
| EXT | 1 | 1 | 0 | Byte code extension | X | - | - | - | - | * | * | - | - | - |
| EXTW | 1 | 2 | 0 | Word code extension | - | X | - | - | - | * | * | - | - | - |
| ZEXT | 1 | 1 | 0 | Byte zero extension | Z | - | - | - | - | R | * | - | - | - |
| ZEXTW | 1 | 2 | 0 | Word zero extension | - | Z | - | - | - | R | * | - | - | - |

Table 25 String Instructions [10 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|--------------|---|--------|----|---|----|----|---|---|---|---|---|---|---|-----|
| MOVS/MOVS | 2 | *2 | *3 | Byte transfer @AH+ \leftarrow @AL+, counter = RW0 | - | - | - | - | - | - | - | - | - | - |
| MOVSD | 2 | *2 | *3 | Byte transfer @AH- \leftarrow @AL-, counter = RW0 | - | - | - | - | - | - | - | - | - | - |
| SCEQ/SCEQI | 2 | *1 | *4 | Byte retrieval @AH+ - AL, counter = RW0 | - | - | - | - | - | * | * | * | * | - |
| SCEQD | 2 | *1 | *4 | Byte retrieval @AH- - AL, counter = RW0 | - | - | - | - | - | * | * | * | * | - |
| FILS/FILSI | 2 | 5m +3 | *5 | Byte filling @AH+ \leftarrow AL, counter = RW0 | - | - | - | - | - | * | * | - | - | - |
| MOVSW/MOVSWI | 2 | *2 | *6 | Word transfer @AH+ \leftarrow @AL+, counter = RW0 | - | - | - | - | - | - | - | - | - | - |
| MOVSWD | 2 | *2 | *6 | Word transfer @AH- \leftarrow @AL-, counter = RW0 | - | - | - | - | - | - | - | - | - | - |
| SCWEQ/SCWEQI | 2 | *1 | *7 | Word retrieval @AH+ - AL, counter = RW0 | - | - | - | - | - | * | * | * | * | - |
| SCWEQD | 2 | *1 | *7 | Word retrieval @AH- - AL, counter = RW0 | - | - | - | - | - | * | * | * | * | - |
| FILSW/FILSWI | 2 | 5m +3 | *8 | Word filling @AH+ \leftarrow AL, counter = RW0 | - | - | - | - | - | * | * | - | - | - |

m: RW0 value (counter value)

*1: 3 when RW0 is 0, $2 + 6 \times (RW0)$ for count out, and $6n + 4$ when match occurs

*2: 4 when RW0 is 0, $2 + 6 \times (RW0)$ in any other case

*3: $(b) \times (RW0)$

*4: $(b) \times n$

*5: $(b) \times (RW0)$

*6: $(c) \times (RW0)$

*7: $(c) \times n$

*8: $(c) \times (RW0)$

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Table 26 Multiple Data Transfer Instructions [18 Instructions]

| Mnemonic | # | cycles | B | Operation | LH | AH | I | S | T | N | Z | V | C | RMW |
|---------------------------|----|--------|----|--|----|----|---|---|---|---|---|---|---|-----|
| MOVM @A, @RLi, #imm8 | 3 | *1 | *3 | Multiple data transfer byte ((A)) ← ((RLi)) | — | — | — | — | — | — | — | — | — | — |
| MOVM @A, eam, #imm8 | 3+ | *2 | *3 | Multiple data transfer byte ((A)) ← (eam) | — | — | — | — | — | — | — | — | — | — |
| MOVM addr16, @RLi, #imm8 | 5 | *1 | *3 | Multiple data transfer byte (addr16) ← ((RLi)) | — | — | — | — | — | — | — | — | — | — |
| MOVM addr16, eam, #imm8 | 5+ | *2 | *3 | Multiple data transfer byte (addr16) ← (eam) | — | — | — | — | — | — | — | — | — | — |
| MOVMW @A, @RLi, #imm8 | 3 | *1 | *4 | Multiple data transfer word ((A)) ← ((RLi)) | — | — | — | — | — | — | — | — | — | — |
| MOVMW @A, eam, #imm8 | 3+ | *2 | *4 | Multiple data transfer word ((A)) ← (eam) | — | — | — | — | — | — | — | — | — | — |
| MOVMW addr16, @RLi, #imm8 | 5 | *1 | *4 | Multiple data transfer word (addr16) ← ((RLi)) | — | — | — | — | — | — | — | — | — | — |
| MOVMW addr16, eam, #imm8 | 5+ | *2 | *4 | Multiple data transfer word (addr16) ← (eam) | — | — | — | — | — | — | — | — | — | — |
| MOVM @RLi, @A, #imm8 | 3 | *1 | *3 | Multiple data transfer byte ((RLi)) ← ((A)) | — | — | — | — | — | — | — | — | — | — |
| MOVM eam, @A, #imm8 | 3+ | *2 | *3 | Multiple data transfer byte (eam) ← ((A)) | — | — | — | — | — | — | — | — | — | — |
| MOVM @RLi, addr16, #imm8 | 5 | *1 | *3 | Multiple data transfer byte ((RLi)) ← (addr16) | — | — | — | — | — | — | — | — | — | — |
| MOVM eam, addr16, #imm8 | 5+ | *2 | *3 | Multiple data transfer byte (eam) ← (addr16) | — | — | — | — | — | — | — | — | — | — |
| MOVMW @RLi, @A, #imm8 | 3 | *1 | *4 | Multiple data transfer word ((RLi)) ← ((A)) | — | — | — | — | — | — | — | — | — | — |
| MOVMW eam, @A, #imm8 | 3+ | *2 | *4 | Multiple data transfer word (eam) ← ((A)) | — | — | — | — | — | — | — | — | — | — |
| MOVMW@RLi, addr16, #imm8 | 5 | *1 | *4 | Multiple data transfer word ((RLi)) ← (addr16) | — | — | — | — | — | — | — | — | — | — |
| MOVMW eam, addr16, #imm8 | 5+ | *2 | *4 | Multiple data transfer word (eam) ← (addr16) | — | — | — | — | — | — | — | — | — | — |
| MOVM bnk : addr16, *5 | 7 | *1 | *3 | Multiple data transfer | — | — | — | — | — | — | — | — | — | — |
| bnk : addr16, #imm8 | | | | byte (bnk:addr16) ← (bnk:addr16) | | | | | | | | | | |
| MOVMW bnk : addr16, *5 | 7 | *1 | *4 | Multiple data transfer | — | — | — | — | — | — | — | — | — | — |
| bnk : addr16, #imm8 | | | | word (bnk:addr16) ← (bnk:addr16) | | | | | | | | | | |

*1: $5 + \text{imm8} \times 5$, 256 times when imm8 is zero.

*2: $5 + \text{imm8} \times 5 + (a)$, 256 times when imm8 is zero.

*3: Number of transfers $\times (b) \times 2$

*4: Number of transfers $\times (c) \times 2$

*5: The bank register specified by "bnk" is the same as for the MOVS instruction.

MB90210 Series

■ ORDERING INFORMATION

| Part number | Type | Package | Remarks |
|-----------------------------------|--|---------------------------------------|----------------|
| MB90214 MB90P214A MB90P214B | MB90214PF MB90P214PF MB90P214BPF | 80-pin Plastic QFP (FPT-80P-M06) | |
| MB90W214A MB90W214B | MB90W214ZF MB90W214BZF | 80-pin Ceramic QFP (FPT-80C-C02) | Only ES level |
| MB90V210 | MB90V210CR | 256-pin Ceramic PGA (PGA-256C-A02) | For evaluation |

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